

# **DESIGN AND STATISTICAL ANALYSIS (MONTECARLO) OF LOW-POWER AND HIGH STABLE PROPOSED SRAM CELL STRUCTURE**

*A Thesis Submitted in Partial Fulfilment  
of the Requirements for the Award of the Degree of*

**Master of Technology  
In  
VLSI Design & Embedded System**

By

**Govind Prasad  
Roll No: 211EC2086**



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**Department of Electronics & Communication Engineering  
National Institute of Technology, Rourkela  
Odisha- 769008, India  
May 2013**

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Under the Supervision of  
**Prof. Debiprasad Priyabrata Acharya**



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**Odisha- 769008, India**

**May 2013**

***Dedicated to my  
mother and father***



**Department of Electronics & Communication Engineering**  
**National Institute of Technology, Rourkela**

**CERTIFICATE**

This is to certify that the Thesis Report entitled “**Design And Statistical Analysis(Monte-Carlo) Of Low-Power And High Stable Proposed SRAM Cell Structure**” submitted by **GOVIND PRASAD** bearing roll no. **211EC2086** in partial fulfilment of the requirements for the award of Master of Technology in Electronics and Communication Engineering with specialization in “**VLSI design and embedded system**” during session 2011-2013 at National Institute of Technology, Rourkela is an authentic work carried out by him under my supervision and guidance. To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other University / Institute for the award of any Degree or Diploma.

Place:

Date:

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## **ABSTRACT**

The reduction of the channel length due to scaling increases the leakage current resulting in a major contribution to the static power dissipation and for stability of the SRAM cell good noise margin is required so noise margin is the most important parameter for memory design. The higher noise margin of the cell confirms the high-speed of SRAM cell. In this work, a novel SRAM cell with eight transistors is being proposed to reduce the static hence total power dissipation. When compared to the conventional 6T SRAM and NC-SRAM cell, the proposed SRAM shows a significant reduction in the gate leakage current, static and total power dissipation while produce higher stability. In the technique employed for the proposed SRAM cell, the operating voltage is reduced in idle mode. The technique led a reduction of 31.2% in the total power dissipation, a reduction of 40.4% on static power dissipation, and The SVN M SINM WTV and WTI of proposed SRAM cell was also improved by 11.17%, 52.30%, 2.15%, 59.1% respectively as compare to 6T SRAM cell and as compare to NC-SRAM cell is 27.26%, 47.44%, 4.31%, 64.44% respectively. It can be found that the proposed cell is taking 28.6% extra area from the conventional SRAM cell whereas it is almost same with NC-SRAM cell. Cadence Virtuoso tools are used for simulation with 90-nm CMOS process technology.

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# TABLE OF CONTENTS

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	Page No.
Acknowledgements .....	1
Abstract .....	2
Table of Content .....	3
List of tables.....	4
List of Figures.....	5
List of Abbreviations.....	6

CHAPTER No	TOPIC	Page No
<b>1</b>	<b>Introduction</b>	<b>9</b>
	1.1 Motivation	10
	1.2 Introduction to Memory Array	11
	1.3 Random Access memory (RAM)	12
	1.3.1 Static Random Access Memory (SRAM)	13
	1.3.2 Dynamic Random Access Memory (DRAM)	13
	1.4 Organisation of thesis	15
<b>2</b>	<b>The Statistical (Monte-Carlo) simulation</b>	<b>16</b>
	2.1 Introduction of Monte-Carlo simulation	17
	2.2 How Statistical Analysis works	17
	2.2.1 Procedure of Monte Carlo on cadence	18
<b>3</b>	<b>Design Strategies and Stability analysis of SRAM Cell</b>	<b>19</b>
	3.1 Design Strategies for SRAM cell	20
	3.1.1 During Data Read Operation	21
	3.1.2 During Data write Operation	22
	3.2 Stability Analysis of SRAM cells	24

<b>4</b>	<b>The Conventional SRAM Cells</b>	<b>29</b>
4.1	The 6T SRAM Cell	30
4.2	Construction of NC- SRAM cell	32
<b>5</b>	<b>The Proposed 8T SRAM Cell</b>	<b>34</b>
5.1	The Cell Structure	35
5.2	Operation of the cell	35
<b>6</b>	<b>Results and Discussion</b>	<b>38</b>
6.1	Transient response	39
6.2	Static and Power Dissipation	40
6.3	Stability Analysis Using N-Curve Method	44
6.4	Statistical Analysis of SRAM cells	47
6.5	Cell Area of SRAM Cells	50
<b>7</b>	<b>Conclusions</b>	<b>53</b>
<b>8</b>	<b>References</b>	<b>54</b>



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## LIST OF TABLES

---

Table No	Title	Page No
1	Delay For Proposed Cell Compared to those of the Conventional SRAM Cells	41
2	Static Power Dissipation of SRAM Cells	44
3	SNM Improvement of the Proposed Cell Compared to that of the Conventional SRAM Cells	47
4	Comparison Of Stability With Monte Carlo Simulation	50
5	Cell Area of SRAM Cells	53

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## LIST OF FIGURES

---

Figure No.	Title	Page No.
1.1	Three transistors DRAM	15
2.1	(a) Normal simulation (b) Monte-Carlo simulation	18
2.2	Step for Monte-Carlo simulation in cadence	19
3.1	6T SRAM Cell during read operation	22
3.2	6T SRAM Cell during write operation	24
3.3	Circuit for WSNM of writing '1'	26
3.4	Circuit for sweeping BL to get write margin	26
3.5	Circuit for sweeping $WL_R$ to get write margin	27
3.6	Circuit for N-curve	28
3.7	Circuit for write margin from WL sweeping	29
4.1	Schematic of 6T SRAM Cell	31
4.2	Schematics of conventional NC-SRAM cell	34
5.1	Schematic of proposed SRAM cell	36
5.2	Schematics of read and write circuits of the SRAM cell and the additional logic for generating the SL signal	37
6.1	Transient Response of Proposed 9T SRAM cell	40
6.2	Total Power waveform of 6T SRAM	42

6.3	Total Power waveform of proposed SRAM	42
6.4	Static Power waveform of 6T SRAM cell	43
6.5	Static Power waveform of proposed SRAM cell	43
6.6	Variation in Power dissipation of SRAM cells at different temperature	44
6.7	6T SRAM cell N-curve	46
6.8	NC SRAM cell N-curve	46
6.9	Proposed SRAM cell N-curve	47
6.10	Monte Carlo simulation of 6T SRAM cell N-curve	48
6.11	Monte Carlo simulation of NC-SRAM cell N-curve	49
6.12	Monte Carlo simulation of proposed SRAM cell N-curve	49
6.13	The histogram of static power dissipation of proposed SRAM cell From 100 point mc-simulation	50
6.14	Layout of 6T SRAM cell	51
6.15	Layout of NC SRAM cell	52
6.16	Layout of proposed SRAM cell	52

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## List of Abbreviations:

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SRAM	Static Random Access Memory
DRAM	Dynamic Random Access Memory
SVNM	Static Voltage Noise Margin
SINM	Current Noise Margin
WTV	Write Trip Voltage
WTI	Write Trip Current
CR	Cell-Ratio
PR	Pull-up Ratio
M-C	Monte-Carlo
BL	Bit-line
WL	Word-line
NC	Novel N control
WWL	Write Word line
RWL	Read Word line
DRV	Data Retention voltage
SL	Select- Line
DVS	Dynamic Voltage Scaling
SNM	Static Noise Margin

# **cHAPTER 1**

## **INTRODUCTION**

## 1.1 Motivation:

Now a day's to reduce the silicon area and to achieve high speed and performance, the devices are being scaled down to a great extent. Supply voltage and size of transistors are the most important parameters as these are the only parameters in the hand of the design engineers. Generally supply voltage is scaled down to reduce the static power dissipation, but along with that for high performance the threshold voltage should also be scaled down. The reduction in the threshold voltage exponentially increases the sub threshold leakage current which leads to increment in the static power dissipation. Static power dissipation is mainly contributed by sub threshold current and gate leakage current [1].

The cache memory in a microprocessor occupies more than 50% of chip area so the leakage power of cache is a major source of power dissipation in the processor [2]. For stability of the SRAM cell static voltage noise margin (SVNM), static current noise margin(SINM),write trip voltage(WTV) and write trip current (WTI) are the most important parameters in memory design. The total leakage power in SRAM cell is determined by the contribution of leakage currents in each transistor of SRAM cell. The leakage current has two main sources, sub-threshold leakage current and gate leakage current (leakage current is dominated by sub-threshold leakage).The band to band tunnelling leakage current is very small for existing Technologies (90nm) and that can be ignored [3]. As the oxide thickness of gate decreases, the gate leakage current of transistor increases exponentially and when gate oxide thickness reaches 3nm and below, the gate leakage current comes to the order of sub-threshold leakage current. It also increases exponentially with voltage across gate oxide.

Considering the BSIM model, the sub-threshold leakage current for a MOSFET device can be expressed as [1]

$$I_{subthreshold} = I_0 e^{\frac{V_{gs} - V_{th}}{\eta V_T}} \left( 1 - e^{\frac{-V_{ds}}{V_T}} \right) \quad (1)$$

Where  $I_0 = \left( \frac{W\mu_0 c_{0x} V_T^2 e^{1.8}}{q} \right) V_T = \frac{KT}{q}$  is the thermal voltage,  $V_{ds}$  and  $V_{gs}$  are the drain to source and gate to source voltage respectively.  $V_{th}$  is the threshold voltage,  $C_{0x}$  is the gate oxide capacitance,  $\mu_0$  is the carrier mobility and  $\eta$  is the sub-threshold swing coefficient.

And the gate leakage current can be modelled by

$$I_{gate} = W.L.A \left( \frac{V_{ox}}{t_{ox}} \right)^2 \exp \left( \frac{-B \left( 1 - \left( 1 - \frac{V_{ox}}{\phi_{ox}} \right)^{3/2} \right)}{\frac{V_{ox}}{t_{ox}}} \right) \quad (2)$$

Where W and L are the width and length of the transistor respectively,

$$A = \left( \frac{q^3}{16 \pi^2 h \Phi_{ox}} \right),$$

$$B = \left( \frac{4\pi \sqrt{2m_{ox}} \Phi_{ox}^{3/2}}{3hq} \right),$$

$m_{ox}$  is the effective mass of the tunnelling particle,  $\phi_{ox}$  is the barrier height,  $t_{ox}$  is oxide thickness, h is plank's constant and q is the electric charge. So For getting low static power an eight-transistor SRAM cell structure is proposed. In this structure, to improve the stability and low power consumption, two transistors are added to the cell, which is achieved at the cost of slight increase in the cell area.

## 1.2 Introduction to Memory Array:

SRAM is a critical component in many of the digital systems, from high-performance processors to mobile-phone chips. In these applications, density, power, and performance are all essential parameters. Earlier, the power for digital logic, which is dominated by

dynamic power, has been reduced by lowering the supply voltage ( $V_{DD}$ ). The supply voltage for Digital circuits has reached around 1 V [4] [5].  $V_{DD}$  scaling down reduces static-noise-margin but increases the transistor mismatch [6]. Besides, there are severe constraints on cell noise margin for reliable read-and-write operation. Also, as device size is scaled, random process variations significantly degrade the noise margin. As the sizing of the SRAM is in nanometer scale the variations in electrical parameters (e.g., threshold voltage, sheet resistance) reduces its steadily due to the fluctuations in process parameters i.e., density of impurity concentration, oxide thickness and diffusion depths [6]. Considering all these effects, the bit yield for SRAM is strongly influenced by  $V_{DD}$ , threshold voltage ( $V_{th}$ ), and transistor-sizing ratios [7]. Therefore, it is complicated to determine the optimal cell design for SRAM. The transistor mismatch can be described as two closely placed identical transistors have important differences in their electrical parameters as threshold voltage ( $V_{th}$ ) [1], body factor and current factor and make the design with less predictable and controllable. The stability of the SRAM cell is seriously affected by the increase in variability and decrease in supply voltage ( $V_{DD}$ ) [8].

### 1.3 Random Access memory (RAM):

Random access memory [9] is a type of computer data storage. It is made of integrated circuits that allow the stored data to be accessed in any order i.e., at random and without the physical movement of storage medium or a physical reading head. RAM is a volatile memory as the information or the instructions stored in the memory will be lost if the power is switched off. The word “random” refers to the fact that any piece of data can be returned at a constant time regardless of its physical location and whether or not it is related to the previous piece of data. This contrasts with the physical movement devices such as tapes, magnetic disks and optical disks, which rely on physical movement of the recording medium or reading head. In these devices, the retrieval time varies with the physical location and the movement time takes longer than the data transfer. The main advantages of RAM over types of storage which require physical movement is that retrieval times are short and consistent. Short because no physical movement is necessary and consistent the time taken to retrieve the data does not depend on the current distance from a physical head. The access time for retrieving any piece of data in RAM chip is same. The disadvantages are its cost compared to the physical moving media and loss of



data when power is turned off. RAM is used as 'main memory' or primary storage because of its speed and consistency. The working area used for loading, displaying and manipulating applications and data. In most personal computers, the RAM is not an integral part of the motherboard or CPU. It comes in the easily upgraded form of modules called memory sticks. These can quickly be removed and replaced when they are damaged or when the system needs up gradation of memory depending on current purposes. A smaller amount of random- access memory is also integrated with the CPU, but this is usually referred to as "cache" memory, rather than RAM. Modern RAM generally stores a bit of data as either a charge in a capacitor, as in dynamic RAM, or the state of a flip-flop, as in static RAM.

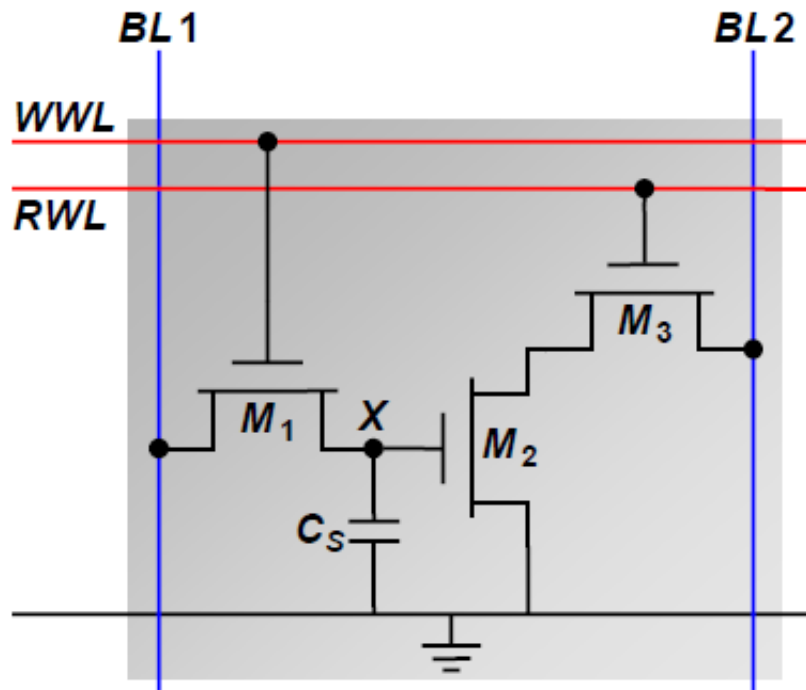
### **1.3.1 Static Random Access Memory (SRAM):**

The word “static” means that the memory retains its contents as long as the power is turned on. Random access means that locations in the memory can be written to or read from in any order, regardless of the memory location that was last accessed. Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. This storage cell has two stable states which are used to denote “0” and “1”. The access transistors are used to access the stored bits in the SRAM during read or write mode. It thus typically takes six MOSFETs to store one memory bit. Access to the cell is enabled by the word line WL which controls the two access transistors  $N_1$  and  $N_2$  which, in turn, control whether the cell should be connected to the bit lines BL and /BL. They are used to transfer data for both read and write operations. The bit lines are complementary as it improves the noise margin.

### **1.3.2 Dynamic RAM (DRAM):**

Dynamic Random Access Memory [10] is a type of RAM that stores each bit of data in a separate capacitor within an integrated circuit. As the capacitors leak charge the circuit needs to be refreshed periodically in order to store the data. The structural simplicity of DRAM as it needs one transistor and one capacitor are required per bit

where as for SRAM it needs six transistors. This criterion allows DRAM to go very high density. It comes in RAM section as it is volatile; it loses data when the power is turned off. The periodic refresh operation consists of a read of the cell contents followed by write operation, should occur often enough that the contents of the memory cells are never corrupted by the leakage. Typically refresh should occur every 1 to 4ms. For a larger memories refresh equipment is placed in the circuit which refreshes every row of the circuit.



**Figure 1.1: Three Transistors Dynamic RAM [10]**

The write operation performed is shown for three transistors Dynamic RAM (Figure1) as the appropriate data value is written on BL1 and asserting the write-word line (WWL). The data is retained as charge on capacitance  $C_s$  once WWL is lowered. When reading the cell, the read-word line (RWL) is raised. The storage transistor  $M_2$  is either on or off depending upon the stored value. The bit line BL2 is pre charged to  $V_{DD}$  before performing read operation. The series connection of  $M_2$  and  $M_3$  pulls BL2 low when a “1” is stored. BL2 remains high in the opposite case. The cell is inverting; that is, the inverse value of the stored signal is sensed on the bit line.

## 1.4 Organization of Thesis:

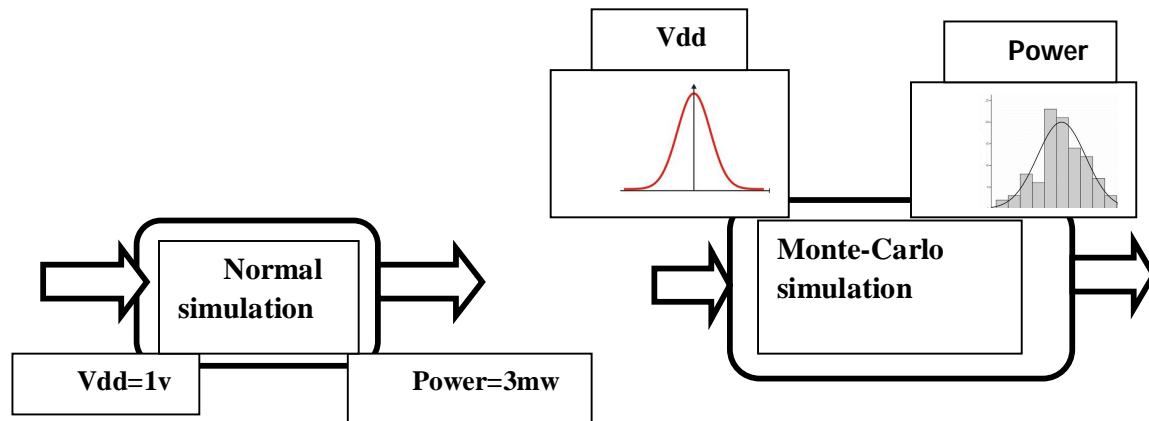
In these thesis I present new techniques based design that reduce the gate leakage current and standby leakage current in the SRAM cells. In this design, we focus on the static power dissipation in the idle mode where the SRAM cell is fully powered on, but no read or write operation is performed the word line is gives low(0) signal to pass transistor . The detailed description of the memory and introduction of thesis is given in the chapter1. The chapter 2 consist detailed description of Monte Carlo simulation. The section 2.1 described about how Monte Carlo simulation works. Chapter 3 of the thesis explains about the Design strategy and stability analysis of the SRAM cell, the section 3.1 described the Design strategy of SRAM cell which is very important for high SNM and low power consumption. The section 3.2 described the stability analysis of SRAM cell, in this section; we introduce five existing static approaches for measuring write margin. The chapter 6 explains about the simulation results and discussions of the SRAM cells. The section 6.1 discusses the transient response of the SRAM cell, section 6.2 discusses the total and static power comparison of conventional and proposed SRAM cell, section 6.3 discusses stability comparisons and section 6.4 Monte Carlo analysis comparison and area comparison discusses in section 6.5. Finally the thesis has been concluded in chapter 7.

## **CHAPTER 2**

# **The STaTiSTical Simul aTion**

## 2.1 Introduction of Monte-Carlo simulation:

The manufacturing variations in components affect the production of any design that includes them. Statistical analysis allows you to study this relationship in detail. In general we can say Monte Carlo simulation is a technique used to understand the impact of risk [11].



**Figure 2.1: (a) Normal simulation (b) Monte-Carlo simulation**

Figure 2.1 (a) and figure 2.1 (b) shows the difference between normal simulation and Monte-Carlo simulation means in normal simulation we are giving fixed supply and we are getting fixed output or power but suppose supply voltage is changed because of some reason then what will be the output or power that we can analysis by Monte Carlo simulation where the shape of each statistical distribution represents the manufacturing tolerances on a device.

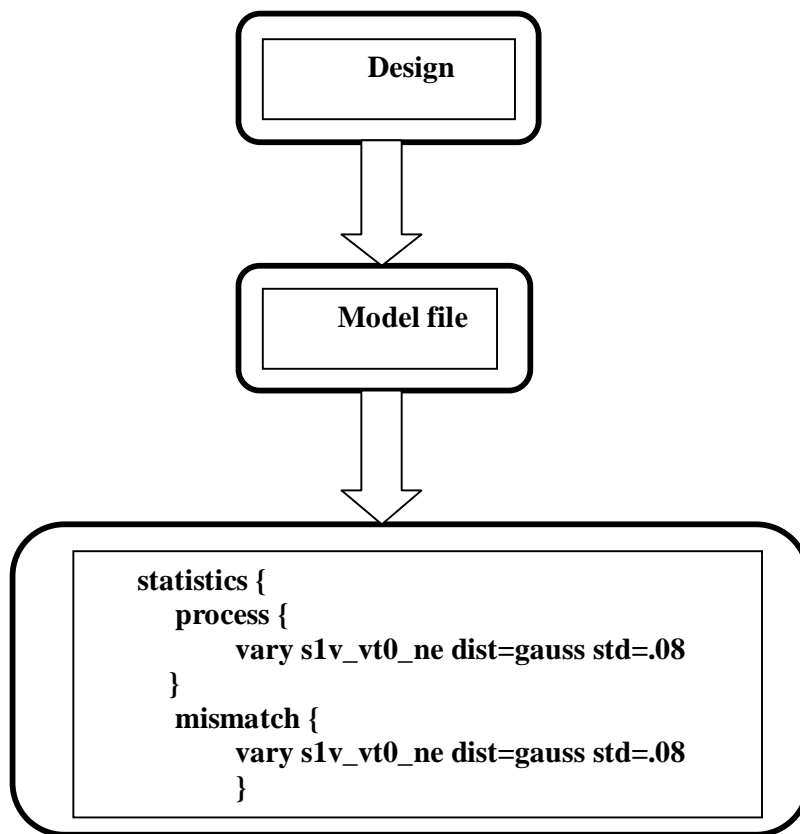
## 2.2 How Statistical Analysis works:

The manufacturing variations in components affect the production yield of any design that includes them. Statistical analysis allows you to study this relationship in detail. To prepare for a statistical analysis, you create a design that includes devices models that are assigned statistically varying parameter values. The shape of each statistical distribution shows the manufacturing tolerances on a device or devices. During the analysis, the statistical analysis option performs multiple simulations, with each simulation using different parameters values for the devices based upon the assigned statistical distributions. When the simulations finish, you can use the data analysis features of the statistical analysis option to

examine how manufacturing tolerances affect the overall production yield of your design. If necessary then you can switch to different components or change the design to improve the yield [12] [13].

### 2.2.1 Procedure of Monte Carlo on cadence:

For Monte Carlo simulation we have to create a Design that includes devices or device models that are assigned statistically varying parameter values.



**Figure 2.2: step for Monte-Carlo simulation in cadence**

The statistics block defines how parameters vary during the analysis. In this case, each parameter has either a Gaussian or a log-normal distribution with a deviation specified by the std parameter. All the parameters vary when process variation is specified and four of them vary when mismatch is specified.

## **CHAPTER 3**

### **DESIGN STRATEGIES AND STABILITY**

#### **ANALYSIS OF SRAM CELL**

### 3.1 Design Strategies for SRAM cell:

To determine the (W/L) ration of the transistors in a SRAM cell two basic requirements must be taken into consideration [14].

- The data read operation on cell should not destroy the stored information in the SRAM cell.
- The SRAM cell should allow modification of the stored information during data-write phase.

Noise margin is the maximum voltage that can be added to the logic gate which not affects the output of logic gate. For stability of the SRAM cell, good SNM is required that is depends on the value of the CR and PR.

CELL RATIO is the ratio between sizes of driver transistor to the load transistor during the read operation.

$$CR = (W_1/L_1) / (W_5/L_5)$$

PULL-UP RATIO is the ratio between sizes of the load transistor to access transistor during write operation.

$$PR = (W_4/L_4) / (W_6/L_6).$$

NM, which affects both, read margin and write margin and also NM related to the threshold voltages of the NMOS and PMOS devices in SRAM cells [15]. For high NM, the threshold voltages of the NMOS and PMOS devices need to be increased. However, the increase in threshold voltage of PMOS and NMOS devices is limited. The reason is that SRAM cells with MOS devices having too much high threshold voltages which is difficult to operate; as it is hard to flip the operation of MOS devices. Changing the Cell Ratio, we got different speed of SRAM cell. If cell ratio increases, then size of the driver transistor also increases, for hence current also increases. As current is an increase, the speed of the SRAM cell also increases. By changing the Cell ratio we got corresponding NM. For different values of CR, we got different values of NM in different technology of SRAM cell. This is same for DRV vs. NM.



### 3.1.1 During Data Read Operation:

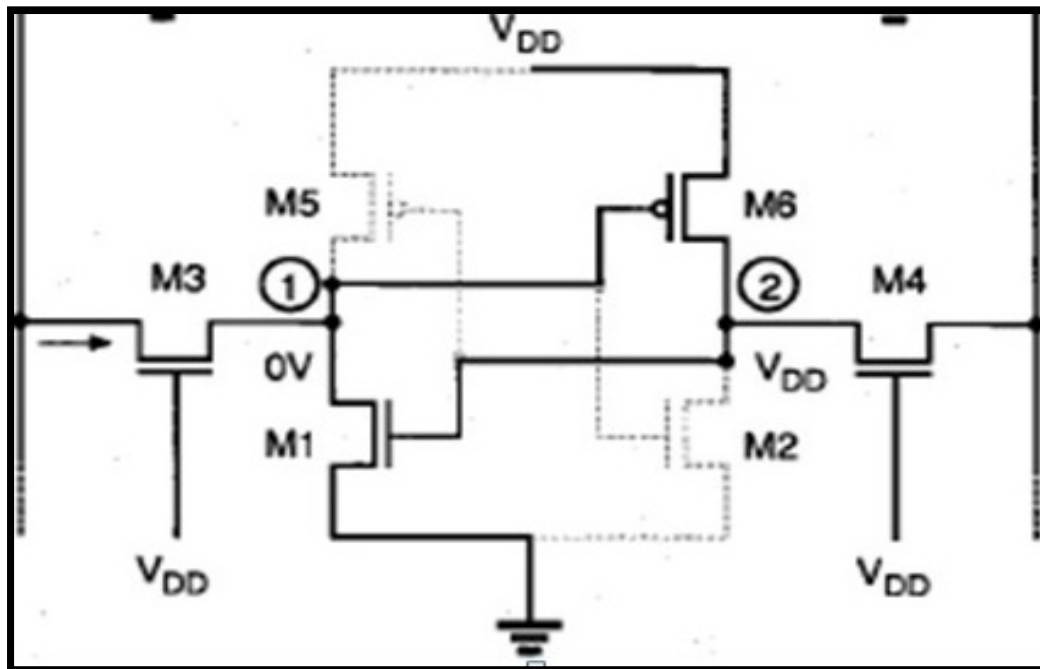


Figure 3.1: 6T SRAM Cell during read operation[14]

When  $M_3$ ,  $M_4$  is turned on the voltage level of column BLB will not show any significant variation since no current will flow through  $M_4$  and  $M_1$  and  $M_3$  will conduct a nonzero current and the voltage level of column BL will begin to drop slightly and the voltage  $V_1$  will increase from its initial value of 0V, where  $V_1$  is the voltage across node 1. If W/L ratio of access transistor  $M_3$  is large compared to the ratio of  $M_1$ , the node voltage  $V_1$  may exceed the threshold voltage of  $M_2$  during this process, forcing an unintended change of the stored state. The key design issue for the data read operation is then to guarantee that the voltage  $V_1$  doesn't exceed the threshold voltage of  $M_2$ , so that  $M_2$  remains turned off during the read phase i.e.,

$$(V_1)_{\max} \leq (V_T)_2$$

For occurring of above condition we have to keep  $M_3$  is in saturation and  $M_1$  is in linear and the current  $I_3$  should be less than equal to  $I_1$

$$I_3 \leq I_1$$

$$\frac{K_{p,3}}{2}(0 - V_{DD} - V_{T,p})^2 \leq \frac{K_{n,1}}{2}(2(V_{DD} - V_{T,n})V_{T,n} - V_{T,n}^2)$$

$$\frac{K_{p,3}}{K_{n,1}} \leq \frac{2(V_{DD} - 1.5V_{T,n})V_{T,n}}{(V_{DD} + V_{T,p})^2}$$

$$\frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_1} \leq \frac{2(V_{DD} - 1.5V_{T,n})V_{T,n}}{(V_{DD} + V_{T,p})^2} \cdot \frac{\mu_n}{\mu_p} \quad (3)$$

Then only we can get the CR range between 1-1.25 that gives maximum range of SNM [14]. Here  $I_3$  and  $I_1$  is the current through transistor M<sub>3</sub> and M<sub>1</sub> respectively.

### 3.1.2 During Data Write Operation:

Now consider the write "0" operation, assuming that logic "1" is stored in the SRAM cell initially. Figure 3.2 shows the voltage levels in the CMOS SRAM cell at the beginning of the data-write operation. The transistors M1 and M6 are turned off, while the transistors M2 and

M5 operate in the linear mode. Thus, the internal node voltages are  $V_1 = V_{DD}$  and  $V_2 = 0$  V before the cell access (or pass) transistors M3 and M4 are turned on.

The column voltage  $V_C$  is forced to logic "0" level by the data-write circuitry; thus, we may assume that  $V_C$  is approximately equal to 0 V. Once the pass transistors M3 and M4 are turned on by the row selection circuitry, we expect that the node voltage  $V_2$  remains below the threshold voltage of M1, since M2 and M4 are designed according to condition.

Consequently, the voltage level at node (2) would not be sufficient to turn on M1. To change the stored information, i.e., to force  $V_1$  to 0 V and  $V_2$  to  $V_{DD}$ , the node voltage  $V_1$  must be reduced below the threshold voltage of M2, so that M2 turns off first. When  $V = V_T$ , the transistor M3 operates in the linear region while M5 operates in saturation.

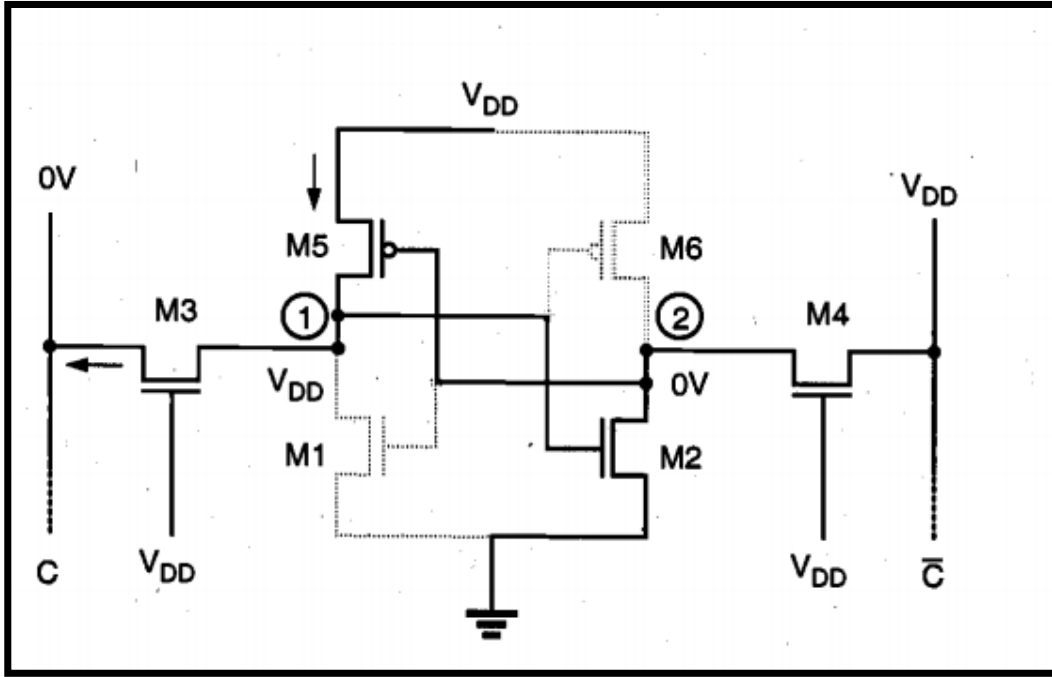


Figure 3.2: 6T SRAM Cell during write operation[14]

$$\frac{K_{p,5}}{2}(0 - V_{DD} - V_{T,p})^2 = \frac{K_{n,3}}{2}(2(V_{DD} - V_{T,n})V_{T,n} - V_{T,n}^2)$$

.....

$$\frac{K_{p,5}}{K_{n,3}} \leq \frac{2(V_{DD} - 1.5V_{T,n})V_{T,n}}{(V_{DD} + V_{T,p})^2}$$

$$\left(\frac{W}{L}\right)_5 \leq \frac{2(V_{DD} - 1.5V_{T,n})V_{T,n}}{(V_{DD} + V_{T,p})^2} \cdot \frac{\mu_n}{\mu_p}$$

(4)

To summarize, the transistor M2 will be forced into cut-off mode during the write "0" operation if condition 4 is satisfied. This will guarantee that M1 subsequently turns on, changing the stored information. Note that a symmetrical condition also dictates the aspect ratios of M6 and M4.

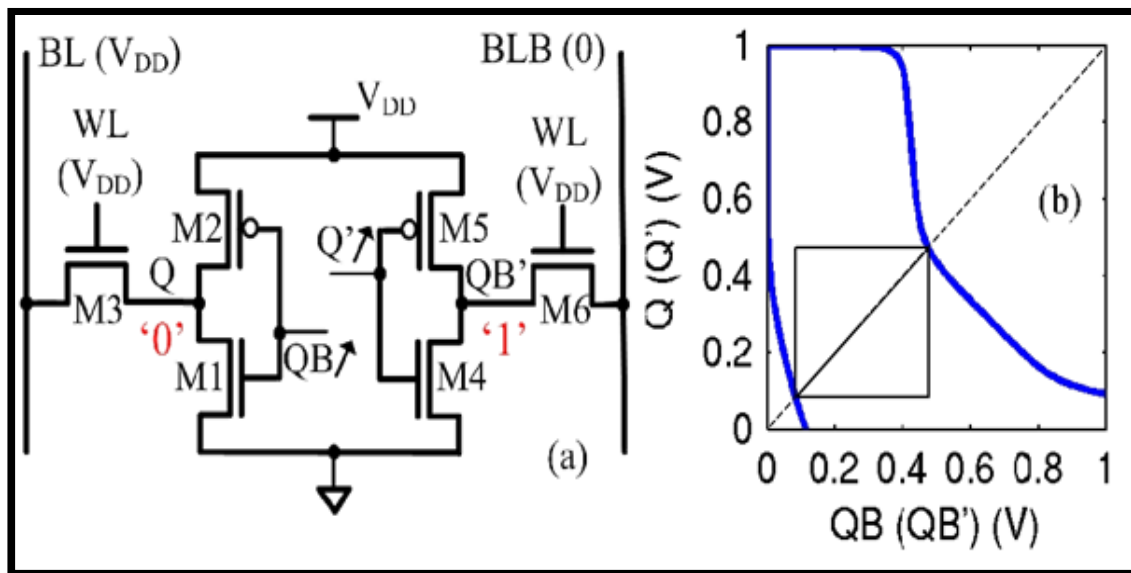
## 3.2 Stability Analysis of SRAM cells:

FOR stability of the SRAM cell good SVN<sub>M</sub> is required so SVN<sub>M</sub> is the most important parameter for memory design. The higher SVN<sub>M</sub> of the cell confirms the high-speed of SRAM. This work is to introduce how the signal to noise margin (SVN<sub>M</sub>), write trip voltage and write trip current of SRAM cell depends on the, cell ratio and pull-up ratio. In order to obtain high noise margin and less power dissipation new SRAM cell have been introduced. PR (pull-up ratio) and CR (cell ratio) and supply voltage are important parameters because these are the only parameters in the hand of the design engineers. Technology is getting more complex day by day so it should be carefully selected in design of the memory cell, there are number of design criteria that must be taken into consideration.

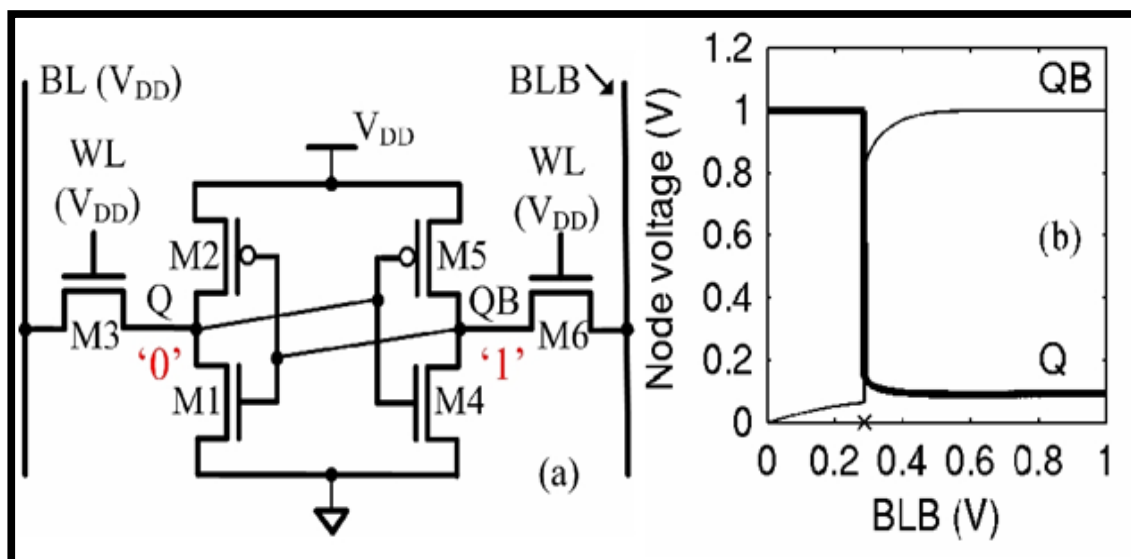
The two basic criteria which we have to taken such as

- Data read operation should not destructive.
- Static noise margin should be in acceptable range.

In this section, we introduce five existing static approaches for measuring write margin. The most common static approach uses SNM as a criterion in Figure 3.3 (a) for a write '1' case. The cell is set in the write operation. Figure 3.3(a) shows the circuit for writing a '1' into the cell. Write SNM (WSNM) is measured using butterfly (or VTC) curves (Figure 3.3(b)), which are obtained from a dc simulation sweeping the input of the inverters (QB and Q'). For a successful write, only one cross point should be found on the butterfly curves, indicating that the cell is mono stable. WSNM for writing "1" is the width of the smallest square that can be embedded between the lower-right half of the curves. WSNM for writing "0" can be obtained from a similar simulation. The final WSNM for the cell is the minimum of the margin for writing '0' and writing '1'. A cell with lower WSNM has write ability.



The BL voltage can also be used as a measure of write margin [17]. The 6T cell is configured is swept downward during simulation. The write margin is defined as the BLB value at the point when Q and QB flip (Figure 3.4(b)), which we will call VBL. The lower that value is, the harder it is to write the cell, implying a smaller write margin.

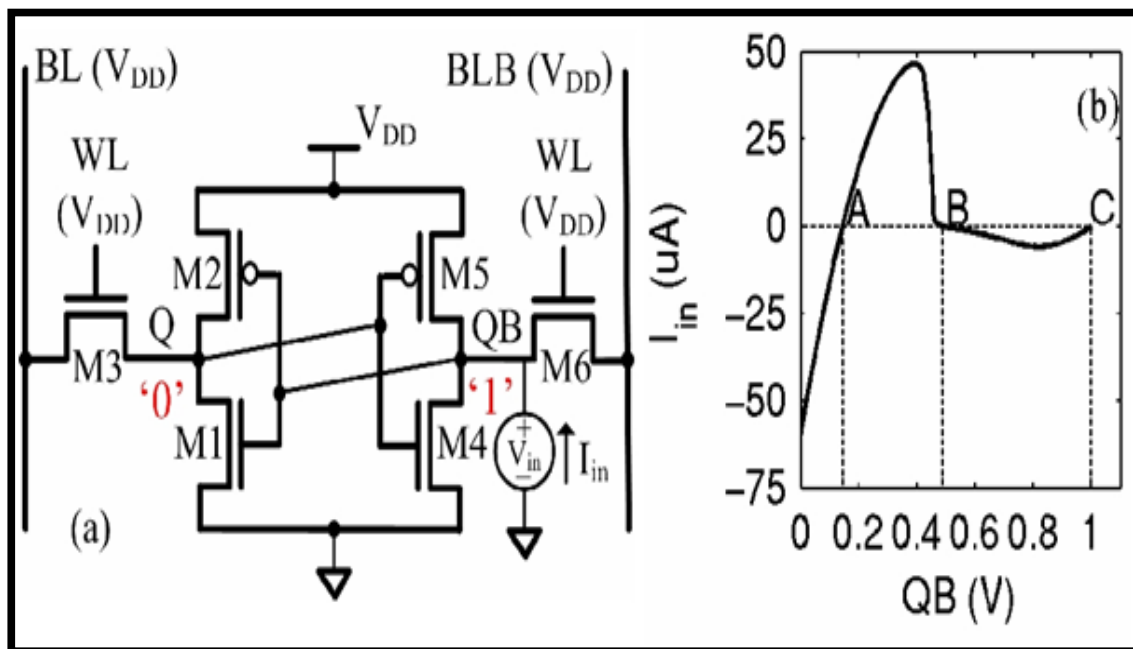


**Figure 3.4: (a) Circuit for sweeping BL to get write margin. (b) Write margin is the BLB value when Q and QB flip. Here the write margin is 0.287V [16]**



from left to right. The curve between C and B is the relevant part for write ability. [20] Defined the voltage difference between C and B as the write trip voltage (WTV), defined the negative current peak between C and B as the write-trip current (WTI), and stated that a higher WTV or WTI implies a smaller

Write margin. It should be noted that WTI actually is the current when VBL reaches the trip point as using the BL method. But these two metrics are not equal. Because of different access transistor strength, cells with the same VBL value might have different WTI values and vice versa. Authors in [20] suggested both WTV and WTI should be evaluated for more accurate write ability analysis, while we find that WTV and WTI are both poorly correlated with write ability.



**Figure 3.6: (a) Circuit for N-curve. (b) WTV is the voltage difference between C and B; WTI is the negative current peak between C and B. Here WTV is 0.511V and WTI is 5.86uA [16]**

The final static method is an improvement over the previous WL method [21]. Instead of only sweeping the WL at the side holding '1', this approach sweeps the WL at both sides simultaneously to replicate a real write operation, where a WL pulse drives both of the access transistors. The write margin is defined as the difference between  $V_{DD}$  and the WL voltage when the nodes Q and QB flip (see Figure 3.7).

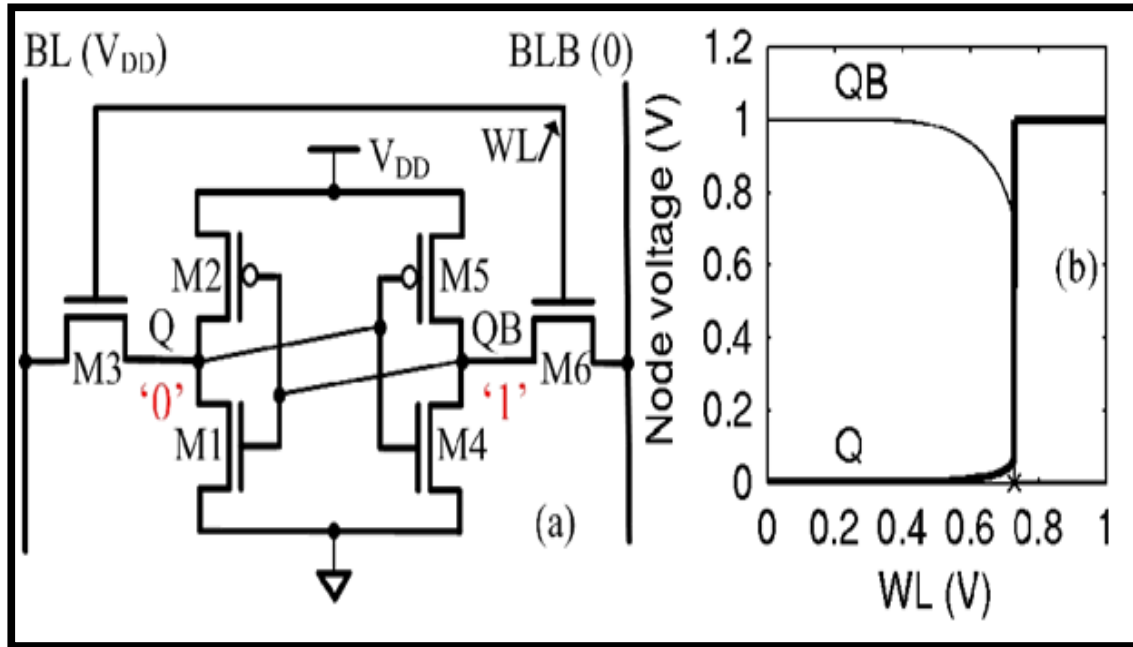


Figure 3.7: (a) Circuit for write margin from WL sweeping. (b) Write margin (VWL) is defined as the difference between  $V_{DD}$  and the WL voltage when the nodes Q and QB flip. For this case, the write margin is 0.272V [16]

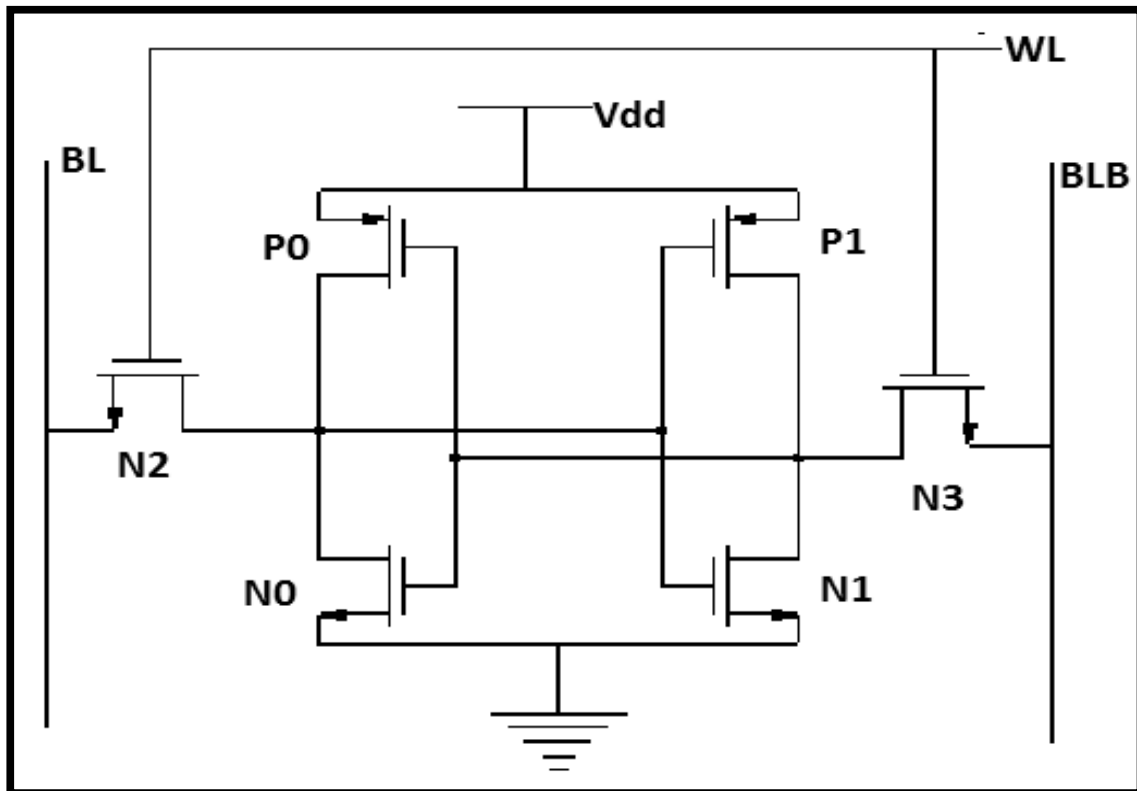


## **CHAPTER 4**

# **THE CONVENTIONAL SRAM CELLS**

## 4.1 The 6T SRAM Cell:

The conventional SRAM cell (6T-SRAM) shown in Figure 4.1, the 6T-SRAM cell has combination of six transistors in which four transistors N0, P0, N1, P1 form back to back connection of inverters to store the single bit either '0' or '1'. For read (write) purpose of data from (to) bit lines, two transistors N2, N3 are used as access transistors. Word line (WL) is used for turn ON and OFF the access transistors. BL, BLB are bit lines [22].



**Figure 4.1: Schematics of conventional 6T SRAM cell**

The conventional SRAM (6T) cell has been found to be rather unstable for deep nano scale technology. This cell fails to meet the so many operational requirements due to the low read static noise margin (SNM). So many configurations have been proposed for improving the stability (SNM) by adding separate structures (read access) to the original 6T SRAM cell configuration. When the conventional SRAM cell is in the read operation, the pass gate is turned on and pulls the node that stores the logic "0" (for example, the node identified by 'qb' in Figure 4.1) to a non-zero value. This decreases the read SNM, especially when a low power supply voltage is utilized. If read SNM is very low and is not acceptable for most

memory designs. To address the reduced read SNM problem, the read and write operations are separated by adding read access structures to the original 6T cell, thus increasing the transistor count to eight. As the read current does not significantly affect the cell value, the read stability of the 8T cell [23] is dramatically increased compared with the original 6T SRAM cell. By using this cell, the read SNM is determined by the two cross-coupled inverters. The worst-case stability condition encountered previously in a 6T SRAM cell is avoided and a high read SNM is retained. Therefore, the 8T cell has a higher read SNM than the 6T SRAM cell. However, for the 8T structure, the read bit line leakage is significant, especially in the deep sub-micron/nano ranges. When the column is not accessed, the leakage current through the read access cell may cause a severe voltage drop at the read bit line, thus errors may appear at the output. Since it has not yet been possible to design a high-density SRAM using 8T cells, this has led to an investigation of other cell configurations such as the 10T structures in [22, 24].

The conventional 6T-SRAM cell has three different modes; standby mode, write mode and read mode. In standby mode no write or read operation is performed which means the circuit is idle, in read mode the data is read from output node to the bit lines and the write mode the data or contents are updated. The SRAM to operate in read mode should have “readability” and write mode should have “write stability”. The three different modes work as follows [25]:

- **Standby:** If the word line WL is low ‘0’ then the access transistors M3 and M4 turn off and the bit lines are disconnected from the inside latch circuit. The cross-coupled inverters will continue to reinforce each other, in this mode the current drawn from supply voltage is called standby or leakage current.
- **Reading:** In read mode the word line WL is high ‘1’, which turns on the transistors N3 and N4, when both the transistors turn on then the value of Q and QB are transferred to BL and BLB bit lines respectively but before giving the WL(1) high the bit lines BL and BLB should be pre-charged to  $V_{DD}$ . Assume that the 1 is stored at Q and ‘0’ at QB so no current flows through N4 and some current is flowing through N3 will discharge the BLB through N3 and N0. This small voltage difference is recognized by sense amplifier that pull the data and produce the output. The decoders (row and column) are used to select the appropriate cell.
- **Writing:** In write mode, suppose we want to write a ‘0’ at the output Q, we would apply a ‘0’ to the bit line means setting BL to ‘0’ and BLB to ‘1’. After setting the bit lines, WL is then asserted.

## 4.2 Construction of NC- SRAM cell :

The NC-SRAM design is based on Dynamic Voltage Scaling (DVS) technique to reduce the leakage current and static power of the SRAM cells and also retains the data stored during the idle mode. The leakage current reduces with operating voltage scaling in deep-submicron processes because of short channel effects [26].

The basic idea of the NC-SRAM is the use of two pass-transistors N4, N5 (Figure 10) that provide different ground supply voltages to the SRAM cell for normal and idle modes [27]. The pass transistor N4 provide a positive voltage when the SRAM cell is in idle mode and another pass transistor N5 provide a virtual ground when the cell is in active mode. The operating voltages of a memory cell are varied to switch between the active and idle (stand-by) modes that will give the less Leakage power significantly [26] [27]. The key idea of the NC-SRAM is the use of two pass-transistors (Fig. 4.2) that provide different ground supply voltages to the memory cell for normal and sleep modes. These pass- transistors provide a positive ground supply voltage when the cell is inactive and connect the cross-coupled inverters to the ground supply during normal operation to function as a conventional 6T-cell. The operating voltages of an array of memory cells are varied to switch between the active and stand-by modes and thus reducing the leakage power significantly. Both the access transistors (M5, M6) are high- $V_t$  devices to further reduce the bit line leakage. Each of the pass gate used to control the source voltages of the NMOS transistors in the cross-coupled inverter is also a high- $V_t$  device to control the leakage current through these two pass transistors (from the positive control voltage  $v$  to ground). None of the nodes is left floating when the cell is not in use and this ensures the stability of the stored data with no additional complexity or circuitry. Since the capacitance of the ground supply lines is significantly less than that of the wells, this approach has improved transition time and energy as compared to others. Moreover, since the source voltage, as opposed to substrate voltage, is used to control the  $V_s$  of the NMOS transistors during the sleep mode, the inherent problems associated with body bias are totally eliminated.

Reduction of the gate leakage current in the SRAM cell has been suggested in [26]. The idea behind the NC-SRAM is to provide different ground levels of the memory cell in active and idle modes. During idle mode the positive voltage more than ground reduces the gate leakage and sub threshold currents of the SRAM cell [26] [27].

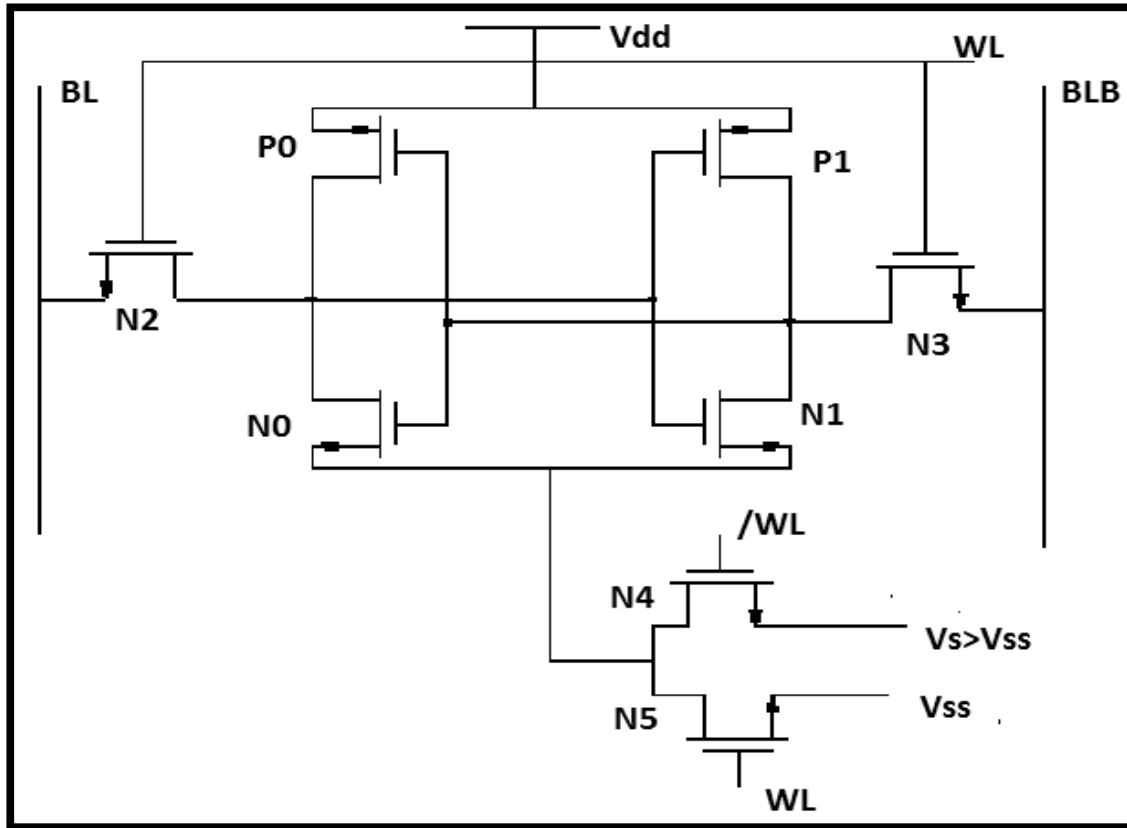


Figure 4.2: Schematic of NC-SRAM Cell

## **CHAPTER 5**

# **The ProPosed 8T srAM Cell I**

## 5.1 The Cell Structure:

The proposed SRAM cell consists of eight transistors five NMOS from N0-N4 and three PMOS from P0-P3 as shown in Figure 5.1. Two transistors N2 and N3 connect the SRAM cell internal node to BLs. Four transistors N0, N1, P0, and P1 form a cross couple structure for data storing purpose. Transistor P2 is for reducing the word line voltage similarly transistor N4 is for reducing the supply voltage and transistor P3 is work as switching transistor.

## 5.2 Operation of the cell:

In Proposed 8T SRAM Cell, during active mode a full supply voltage  $V_{DD}$  is applied to SRAM but during inactive mode or in standby mode a reduced supply voltage of  $V_D$  is applied. Since transistor P1 is in ON state, the drain voltages of transistors N0 and N1 are also at  $V_D$ , the value of  $V_D$  is less than  $V_{DD}$  So The gate leakage currents of transistors N0 and N1 get reduced because gate leakage currents is depend on the gate-source and gate-drain

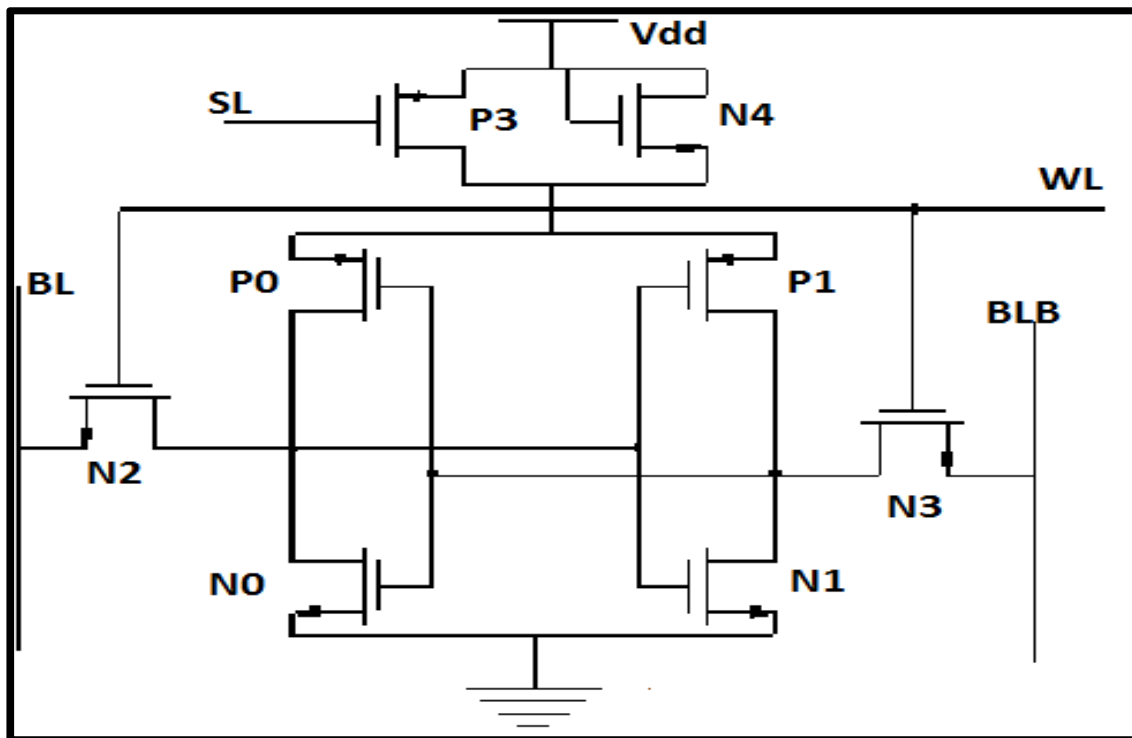
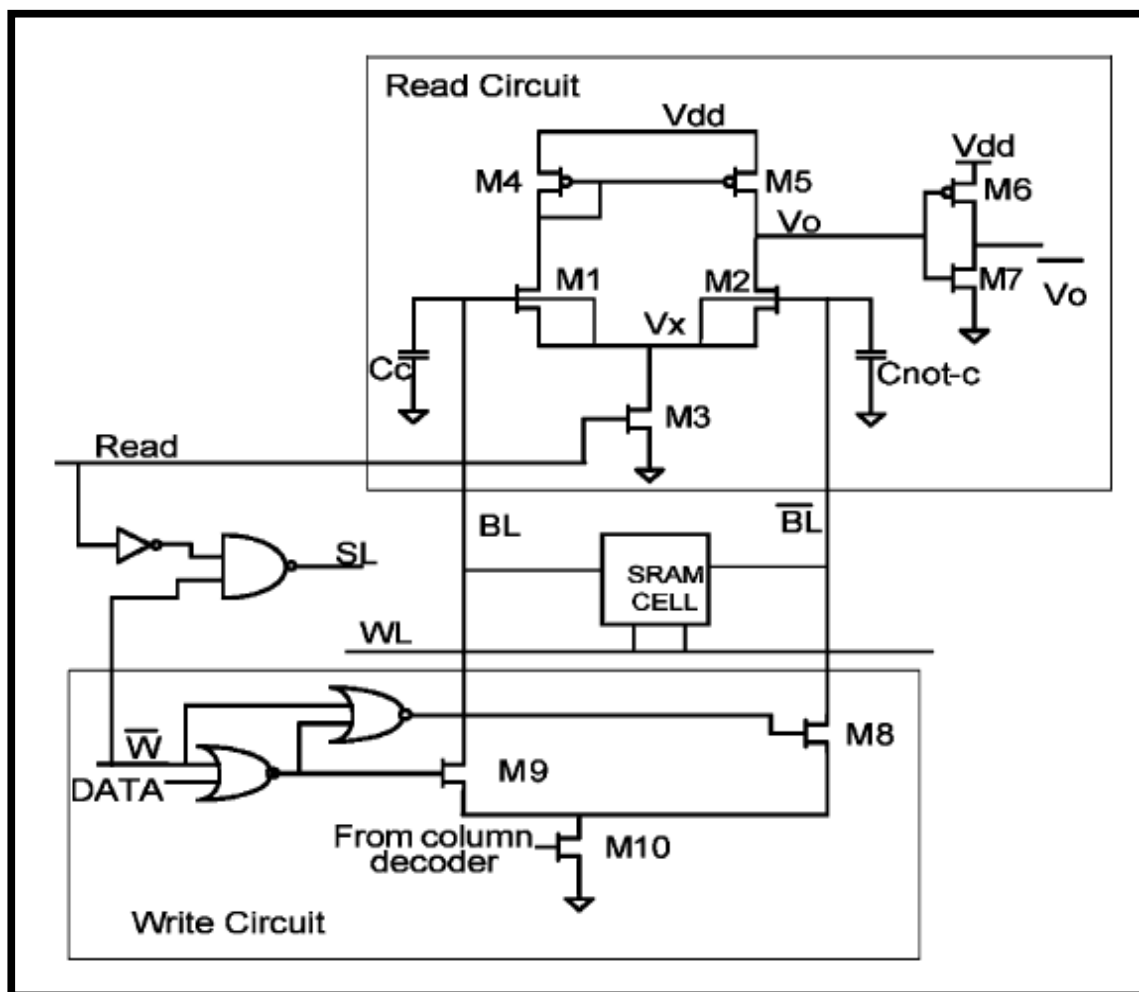


Figure 5.1: Schematic of proposed SRAM cell

Voltage of transistor and here the gate-drain voltage of N1 and gate-source voltages of NO are reducing. Also a decrease in drain voltage of transistor N3 gives a less gate leakage current through it. The gate leakage current through transistor N2 remains unchanged. The sub-threshold leakage currents are reduced in Transistors P1 but remain unaltered in N1. Further, a new sub-threshold leakage current appears in N3 due to the reduction in drain voltage of transistor. This additional sub-threshold leakage current through N3 transistors can be reduced by making the floating bit lines. Hence, above approach is successful in reducing the gate leakage currents of transistors.



**Figure 5.2: Schematics of read and write circuits of the SRAM cell [28] and the additional logic for generating the SL signal.**



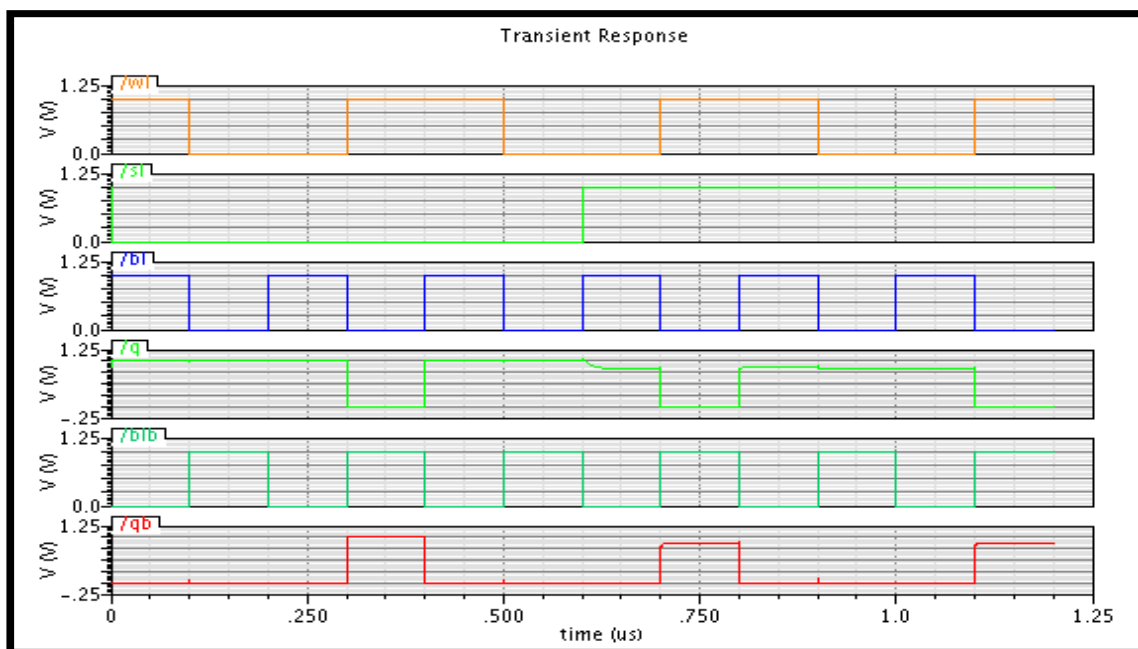
To improve the timing performance of the proposed 8TSRAM cell, instead of using WL and /WL in the proposed 8TSRAM cell, we use SL signal to change the supply level sooner during the active mode. Figure 5.2 shows the proposed 8T SRAM cell. In the read/write mode, WL (word line) and SL (select line) are high and low respectively while in the idle mode, WL and SL are low and high respectively. In this configuration, the SL is always activated before WL is activated. This will give the minimum delay in the write and read Operations compared to conventional SRAM cell. Here for SRAM cell many control signals are used for different operation (read, write, idle) at different times [28] [29]. Here we are using the control signal SL for switching the SRAM cell from active mode to idle mode so for generating the first control signal SL, we use the read and /w signal in the SRAM signal as shown in fig4. In above figure the read and write circuit is shown separately so for write mode the data is applied to SRAM cell when /w is active while for read mode the data is ready for read operation when read signal is activated. For both read and write operations, /W and read signals are activated before the WL is activated and hence the size of P3 should not be very large as compare to others transistor to avoid the delay of read and write operation. When control signal SL become low, transistor P2 turns on taking  $V_A$  (voltage across point A) equal to  $V_{DD}$  but when control signal SL become high then the transistor P2 turns off and the  $V_A$  (voltage across point A) become  $V_D$  and the value of  $V_D$  is less than the supply voltage  $V_{DD}$ .

## **CHAPTER 6**

# **RESULTS AND DISCUSSION**

## 6.1 Transient response:

Now we will discuss the transient response of the proposed SRAM cell, the timing diagrams in the write mode of proposed SRAM cell is shown in Figure 6.1 for a 1 V and 90nm technology, where the WL (word line) transition is considered as reference time. Suppose at time 300.508ns , the signal WL is activated to select the data and after 300.783ns, the writing of the new data is finalized, means the SRAM cell has take 27.5ps for restoring the data.



**Figure 6.1: Transient Response of Proposed 9T SRAM cell**

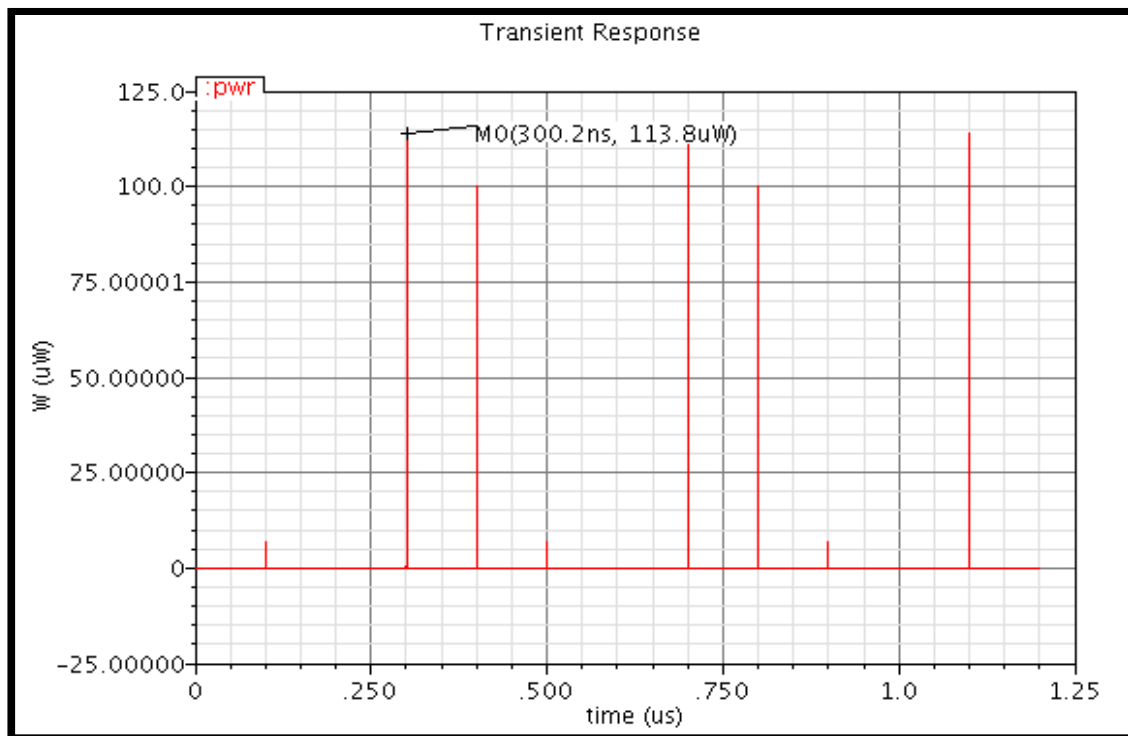
The write delay increases for proposed cell compared to those of the conventional cell are reported in Table I. Compared to the conventional 6T- SRAM cell, the performances of the read and write operations in NC-SRAM, and proposed SRAM cells are degraded. Two extra NMOS transistors are present in the NC-SRAM, because of using two extra NMOS transistors, through that a virtual ground is conferred to the SRAM cell; the write time is degraded by 4.3%. In the proposed SRAM cell, the write access time is deteriorated by 2.42%.

**TABLE I:**  
**DELAY FOR PROPOSED CELL COMPARED**  
**TO THOSE OF THE CONVENTIONAL SRAM CELLS**

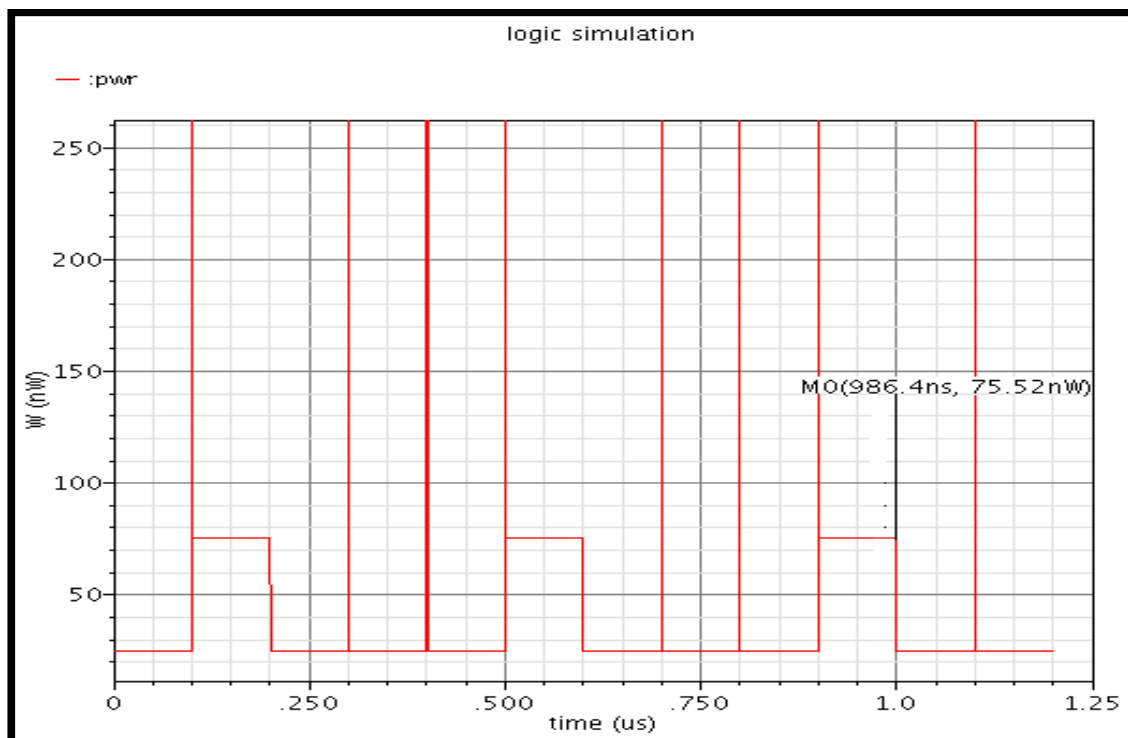
SRAM CELL	6T-SRAM	NC-SRAM	PROPOSED SRAM
DELAY	17.9ps	24.12ps	27.5ps

## 6.2 Static and Power Dissipation:

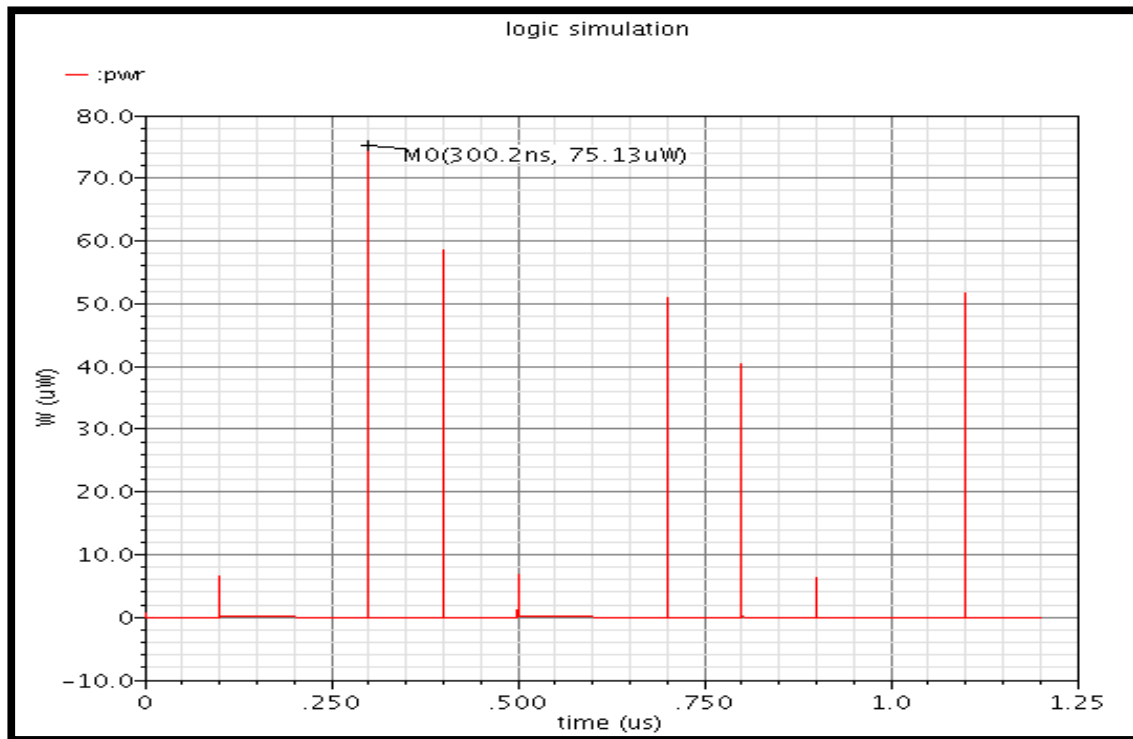
To evaluate the static power dissipation, and stability (SVNM, SINM, WTV, and WTI) of the SRAM cells, we performed simulation for 90-nm technology with temperatures of  $27^{\circ}C$  and supply voltage of  $V_{DD}=1V$  and the channel length  $L=100nm$ , width  $W$  of NMOS and PMOS are fixed at  $120nm$ . Simulation waveform of the total power dissipation for the 6T-SRAM cell and proposed SRAM are shown in Figure 6.2 and Figure 6.4 respectively similarly for static power shown in Figure 6.3 and Figure 6.5 respectively, as from simulation results, the static power dissipation of the proposed structure is reduced by almost 40.4% compared to that of the conventional 6T-SRAM cell and 12.4% compare to NC-SRAM cell. The total power dissipation of the proposed SRAM cell is also reduced by almost 31.24% compared to that of the conventional 6T-SRAM cell and 10.4% compare to NC-SRAM cell. The static power dissipation decreases for proposed cell compared to those of the conventional 6T SRAM cell and NC-SRAM are reported in Table II. Compared to the conventional 6T- SRAM cell and NC-SRAM cell, the static power dissipation of proposed SRAM cell is reduced.



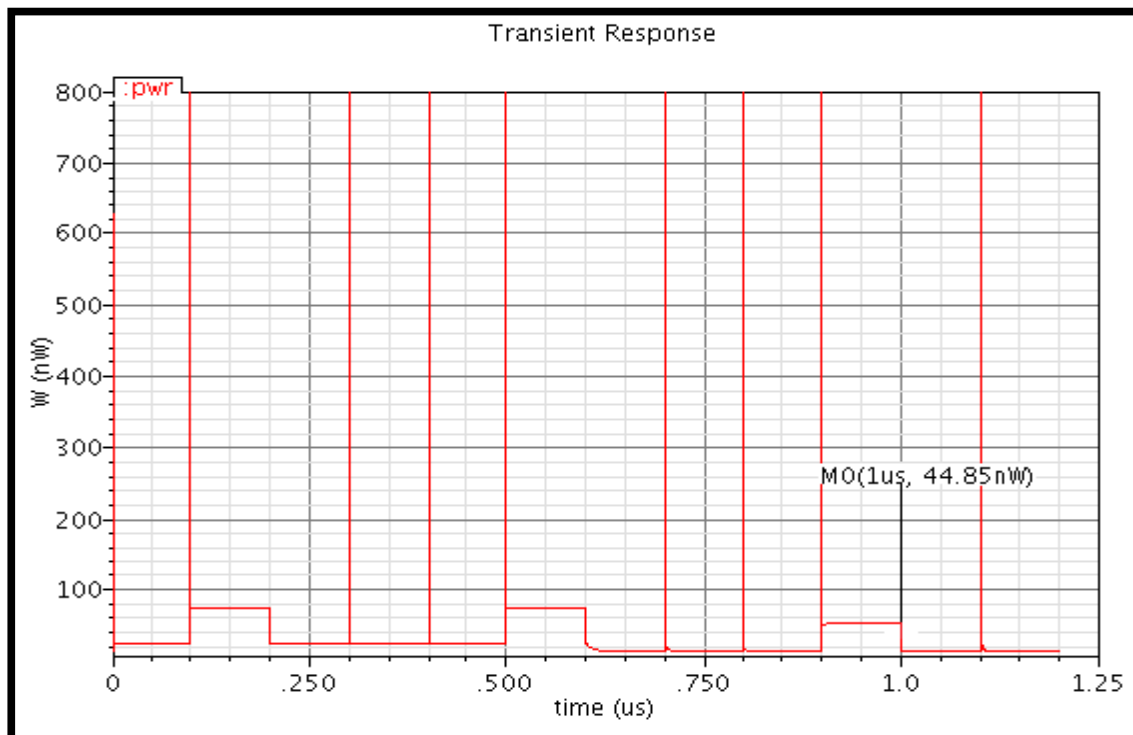
**Figure 6.2: Total Power waveform of 6T SRAM**



**Figure 6.3: Static Power waveform of 6T SRAM cell**



**Figure 6.4: Total Power waveform of proposed SRAM**

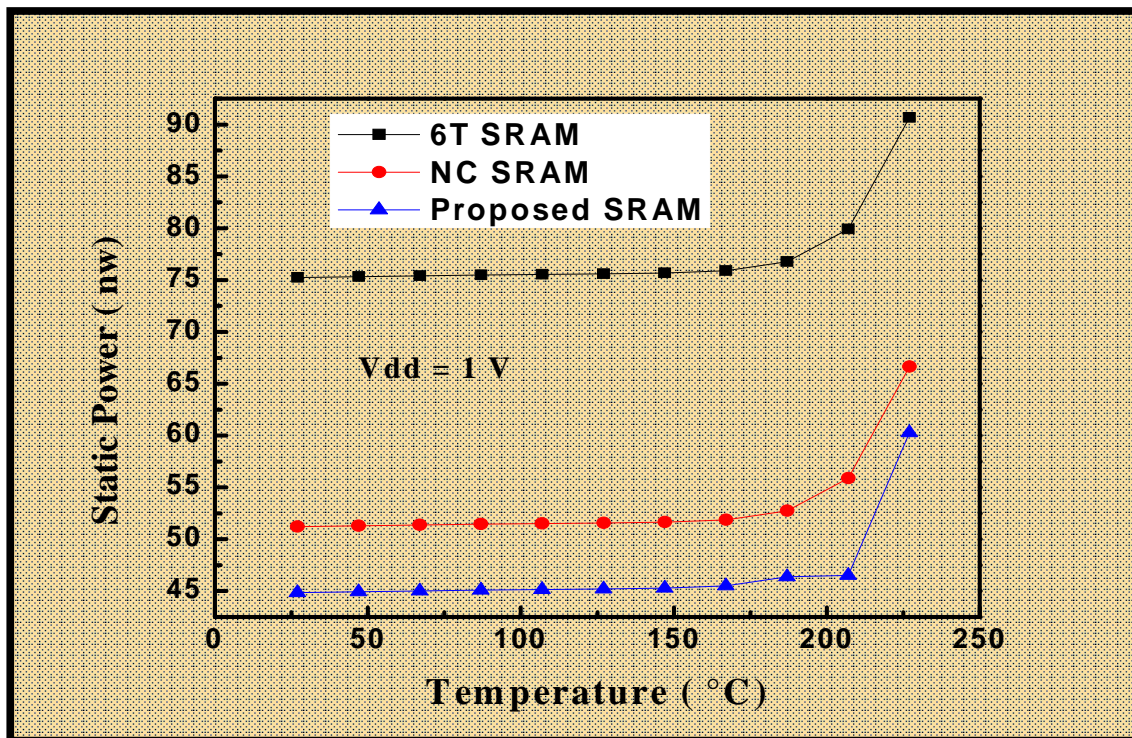


**Figure 6.5: Static Power waveform of proposed SRAM cell**

**TABLE II:**  
**STATIC POWER DISSIPATION OF SRAM CELLS**

<b>SRAM CELL POWER</b>	<b>6T-SRAM</b>	<b>NC-SRAM</b>	<b>PROPOSED SRAM</b>
<b>STATIC POWER DISSIPATION</b>	75.24nW	51.21nW	44.85nW
<b>TOTAL POWER DISSIPATION</b>	667.6uW	512.2uW	459uW

The static power dissipations for all the three SRAM cells at the different temperature are shown in Figure 6.6. From literature review we know that the gate leakage current does not depend much on the temperature but the sub-threshold leakage current is a strong function of temperature. Hence static power dissipation is a strong function of temperature which is shown in figure 6.6.



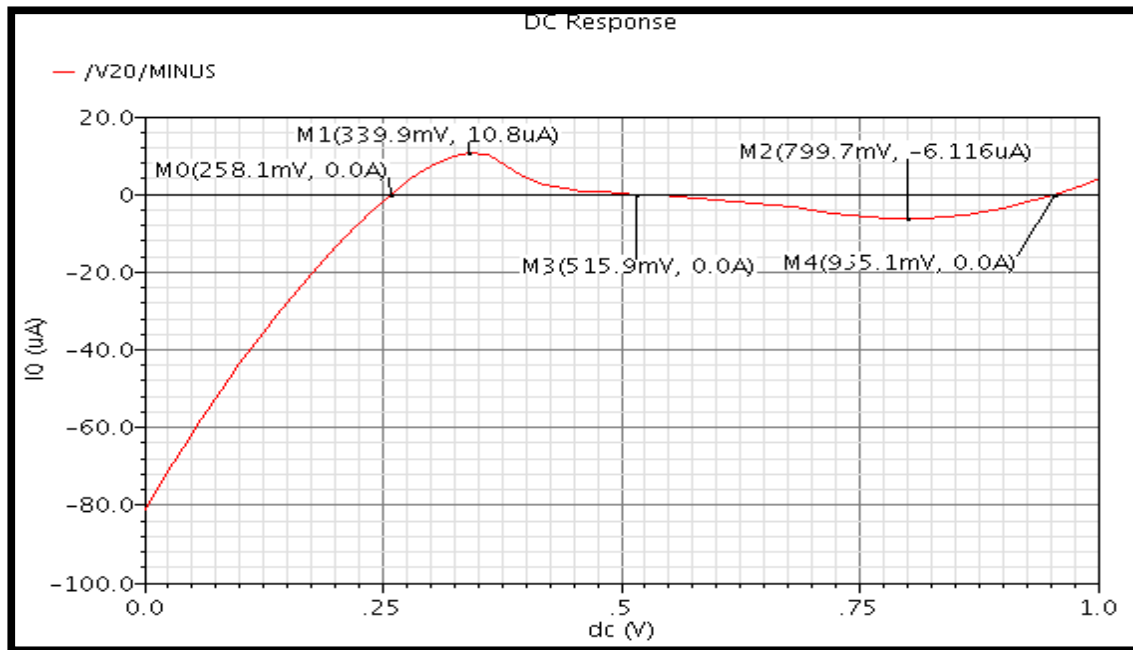
**Figure 6.6: Variation in Power dissipation of SRAM cells at different temperature**

### 6.3 Stability Analysis Using N-Curve Method:

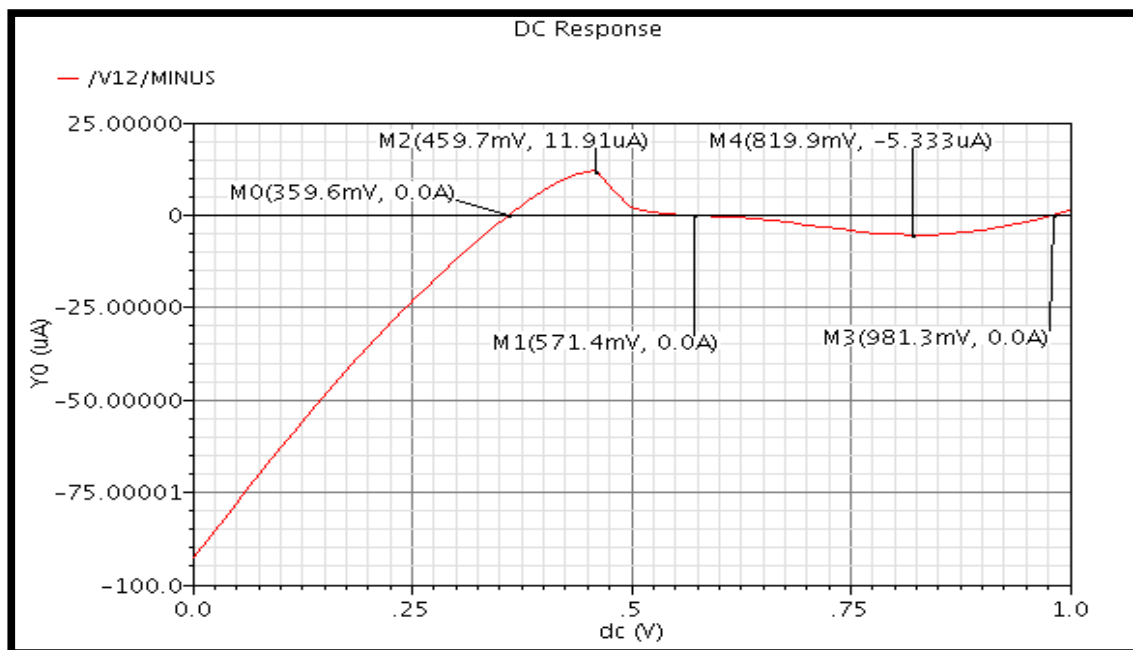
Normally the stability of the SRAM cell is defined by the Static Noise Margin (SNM) and the Write Trip Point (WTP). SNM is defined as the maximum value of DC noise voltage that can be tolerated by the cell without changing the output or stored bit. So the cell stability depends on supply voltage, as supply voltage is reduced the cell becomes less stable. The most common static approach for measuring the SNM is by using butterfly (or VTC) curves, which are obtained from a DC simulation. The disadvantage of measuring the SNM using butterfly curves is the inability to measure the SNM with automatic inline testers, as after measuring the butterfly curves the static noise margin still has to be derived by mathematical calculation of measured data of the SRAM cell. So for inline testers here N-Curve analysis is used for analysis of SRAM cells [30]. N-curve gives both information voltage and current as shown in Figure 6.7 and allows scaling described for the SNM. The curve crosses zero at three points E, G and H from left to right. The voltage difference between point E and G is called static voltage noise margin (SVNM), the curve between point G and H shows the write ability so the voltage difference between point G and H is called write trip voltage (WTV), the peak current located between point E and G means at point F is called static current noise margin (SINM) and the negative current peak between point G and H is called write trip current (WTI). So N-curve analysis gives additional information as compared to butterfly curve analysis.

The stability increases for the proposed cell compared to those of the conventional 6T SRAM cell and NC-SRAM are reported in Table III. Compared to the conventional 6T-SRAM cell and NC-SRAM cell, the stability of the proposed SRAM cell is increased.

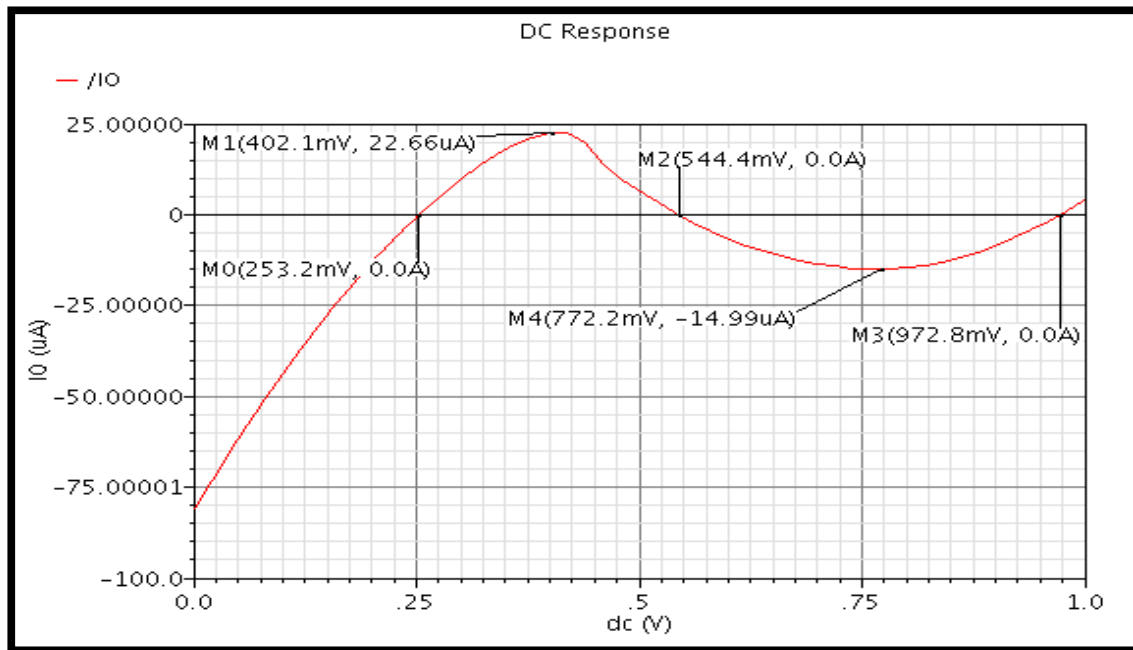




**Figure 6.7: 6T SRAM cell N-curve**



**Figure 6.8: NC SRAM cell N-curve**



**Figure 6.9: Proposed SRAM cell N-curve**

**TABLE III**

**SNM IMPROVEMENT OF THE PROPOSED CELL COMPARED  
TO THAT OF THE CONVENTIONAL SRAM CELLS**

	Conventional SRAM 6T	NC-SRAM	PROPOSED SRAM
CMOS PROCESS	90nm /1V	90nm /1V	90nm /1V
SVNM	257.8mV	211.8mV	291.2mV
SINM	10.8uA	11.91uA	22.66uA
WTV	419.2mV	409.9mV	428.4mV
WTI	-6.12uA	-5.33uA	-14.99uA

## 6.4 Statistical Analysis of SRAM cells:

A family-of-curves shows the superimposed waveforms generated during all of the statistical analysis iterations. This kind of plot illuminates the variability introduced in waveform variables by process and mismatch variations. The Waveform window opens with the overlapping waveforms, depending on the number of iterations included here the M-C simulation(family-of-curves) of 6T-SRAM,NC-SRAM and proposed SRAM cell is shown in Figure 6.10, Figure 6.11 and Figure 6.12 respectively, where the number of iterations (N) is 100 and supply voltage is 1V. Figure 6.12 shows that in the voltage range of about .25 to .50V, the value of current is affected by the statistical analysis variations introduced in the NMOS and PMOS is more. If this voltage range is critical, then we have to redesign our circuit so that the variation is smaller in this range. The comparison of stability (SVNM, SINM, WTV, and WTI) at normal simulation and Monte-Carlo simulation for the proposed cell compared to those of the conventional 6T SRAM cell and NC-SRAM are reported in Table IV.

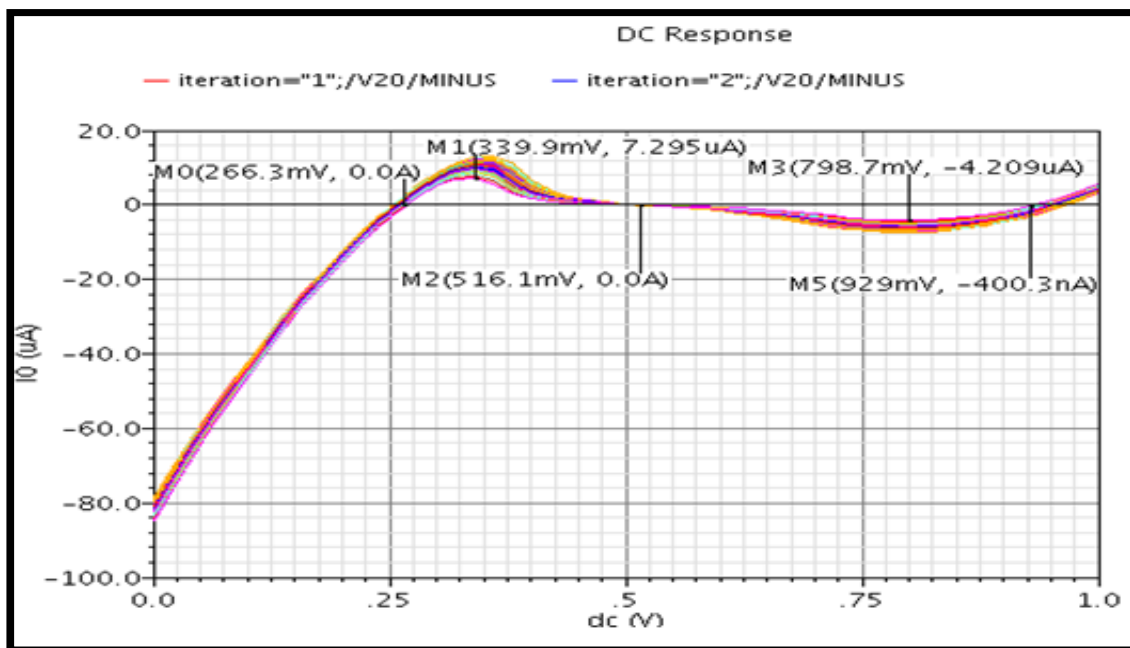


Figure 6.10: Monte Carlo simulation of 6T SRAM cell N-curve

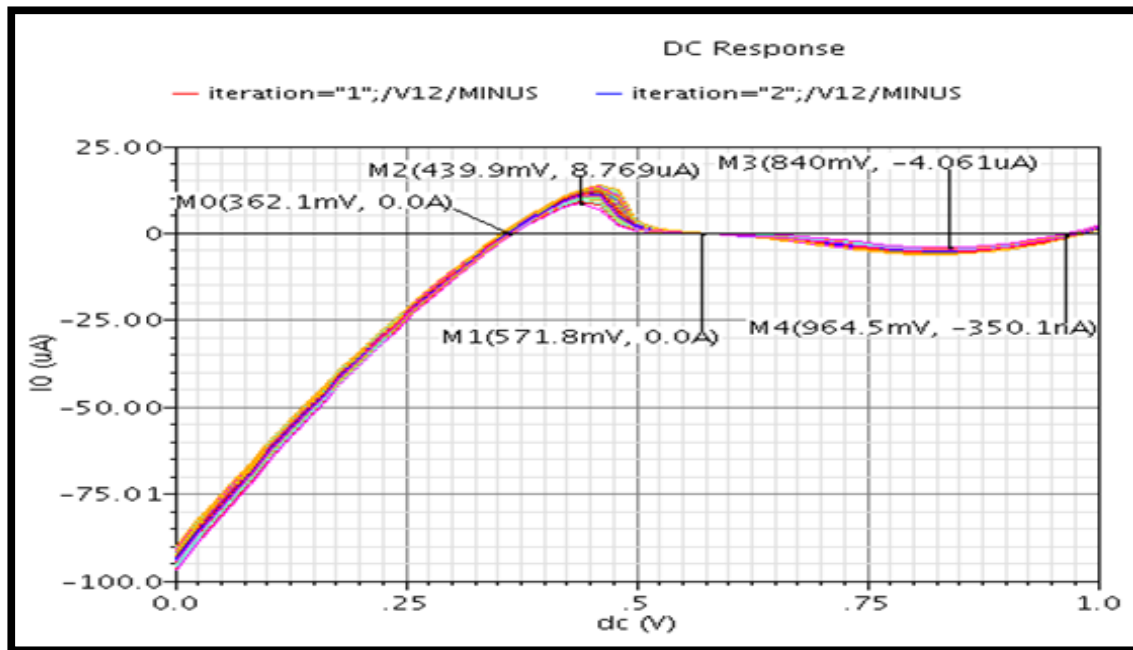


Figure 6.11: Monte Carlo simulation of NC-SRAM cell N-curve

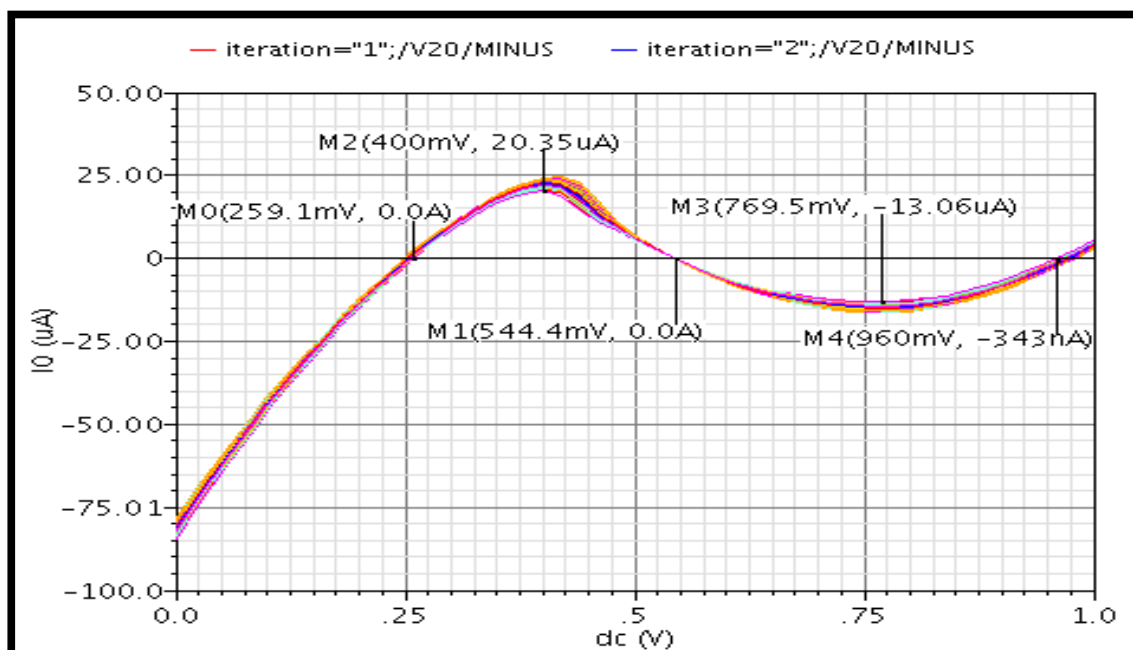
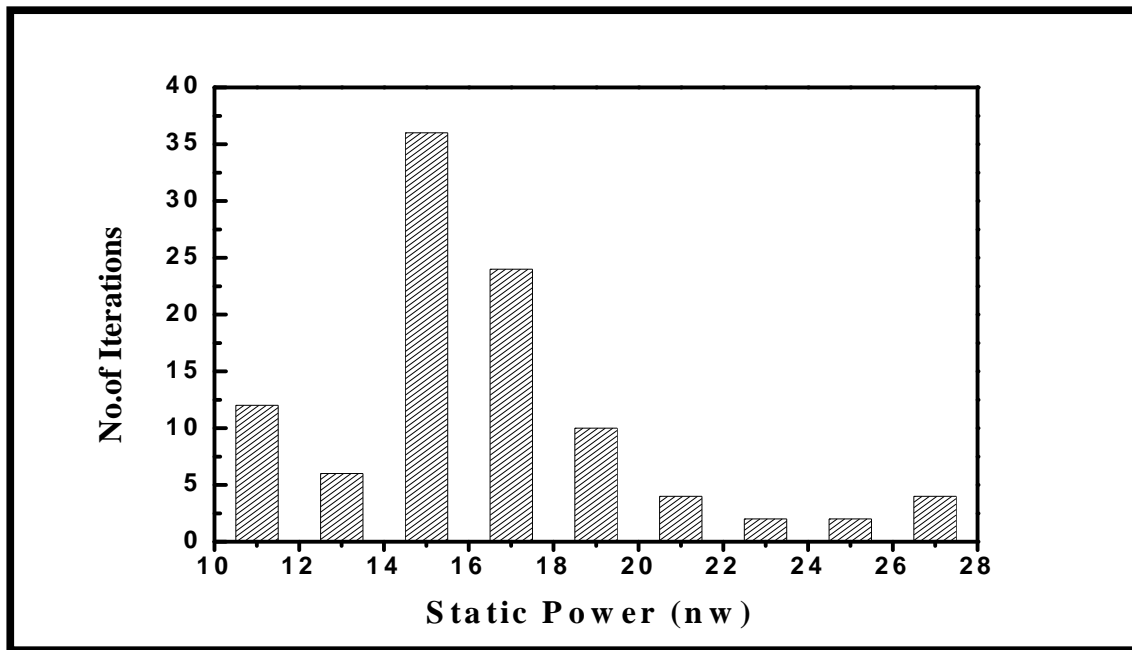


Figure 6.12: Monte Carlo simulation of proposed SRAM cell N-curve

**TABLE IV**  
**COMPARSION OF STABILITY WITH MONTE CARLO SIMMULATION**

<b>SRAM CELL SIMMULATION</b>		<b>6T-SRAM</b>	<b>NC-SRAM</b>	<b>PROPOSED SRAM</b>
<b>NORMAL SIMMULATIM</b>	SVNM	257.8mV	211.8mV	291.2mV
	SINM	10.8uA	11.91uA	22.66uA
	WTV	419.2mV	409.9mV	428.4mV
	WTI	-6.11uA	-5.33uA	-14.99uA
<b>MONTE-CARLO SIMMULATION</b>	SVNM	249.8mV	209.7mV	285.3mV
	SINM	7.295uA	8.769uA	20.35uA
	WTV	412.9mV	392.7mV	415.6mV
	WTI	-4.20uA	-4.06uA	-13.06uA

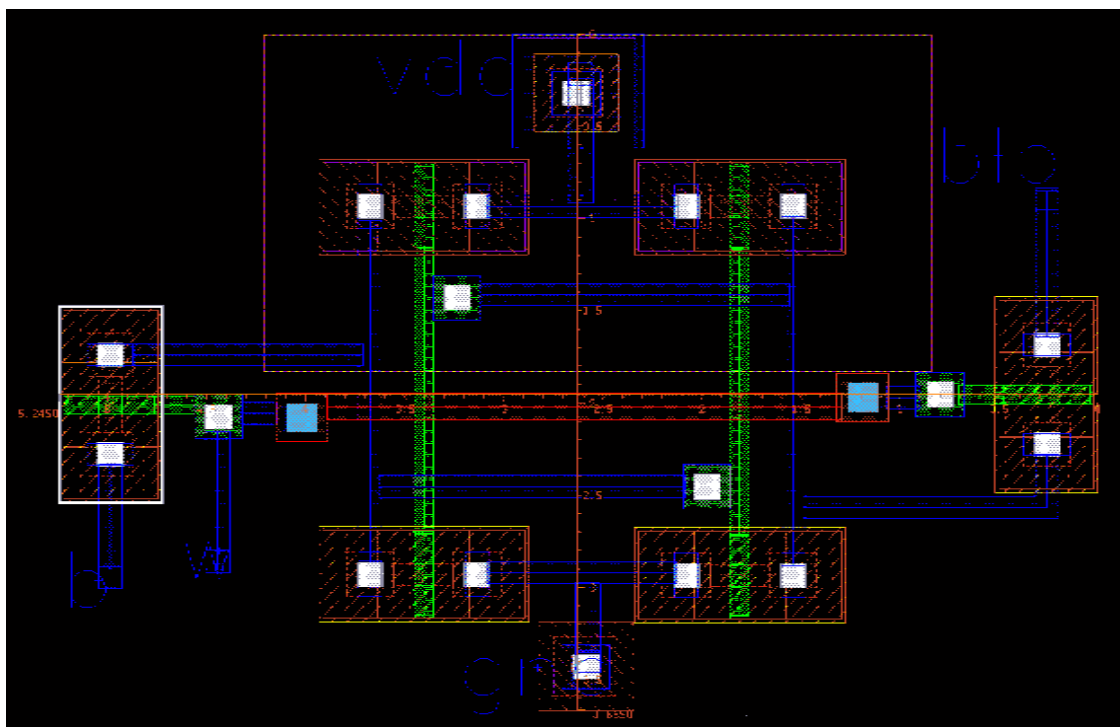


**Figure 6.13: The histogram of static power dissipation of proposed SRAM cell from  
100 point mc-simulation**

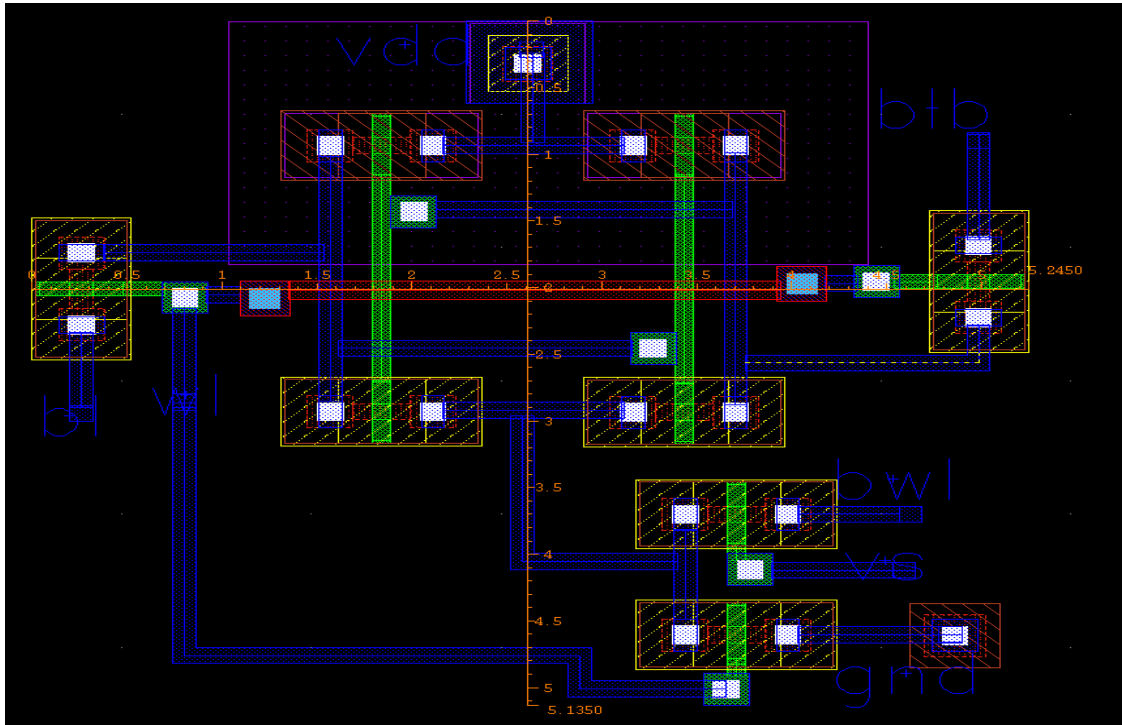
Figure 6.13 shows the histogram for static power dissipation during the Monte Carlo simulation. The x-axis shows the range of static power dissipation and the y axis shows its number of occurrence.

### 6.5 Cell Area of SRAM Cells:

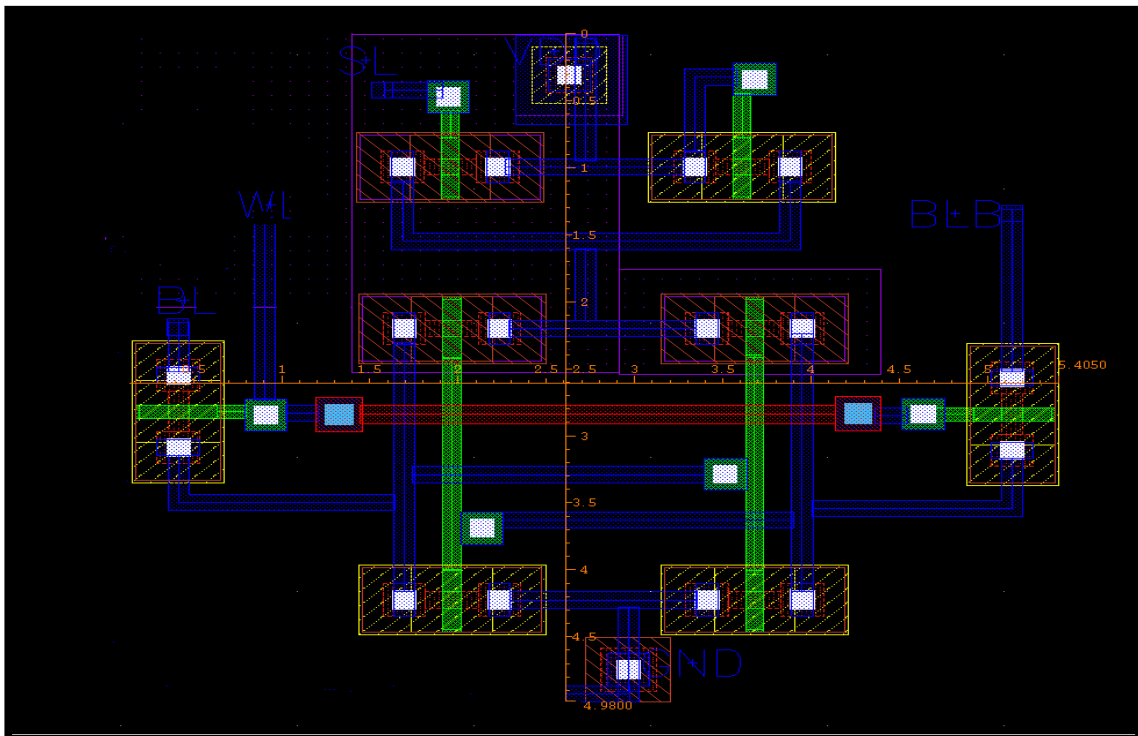
Figure 6.14, Figure 6.15, Figure 6.16 shows the layouts of conventional 6T-SRAM, NC-SRAM and proposed SRAM cells drawn in CMOS technology (using 90-nm).



**Figure 6.14: layout of 6T SRAM cell**



**Figure 6.15: layout of NC SRAM cell**



**Figure 6.16: layout of proposed SRAM cell**

Table V represents the cell area of conventional SRAM, NC-SRAM and the proposed SRAM cell. It can be found that the proposed cell is taking 28.6% extra area from the conventional SRAM cell whereas it is almost same with NC-SRAM cell.

**TABLE V:**  
**CELL AREA OF SRAM CELLS**

<b>SRAM CELL AREA</b>	<b>6T-SRAM</b>	<b>NC-SRAM</b>	<b>PROPOSED SRAM</b>
<b>CELL AREA</b>	19.22 $\mu\text{m}^2$	26.93 $\mu\text{m}^2$	26.92 $\mu\text{m}^2$



## **CHAPTER 7**

## **CONCLUSIONS**

## 7 Conclusions:

In this thesis, I present detailed simulation results for Proposed SRAM in 90nm technology and supply voltage is 1V. Here first, we present the static and total power savings obtained in Proposed SRAM design as compared to the conventional 6T and NC-SRAM cell, Second we present SVN, SINM, WTV and WTI of the Proposed 9T-SRAM design using N-curve analysis and the comparison of stability (SVNM, SINM, WTV, and WTI) at normal simulation and Monte-Carlo simulation for the proposed cell compared to those of the conventional 6T SRAM cell and NC-SRAM. The percentage savings in static power dissipation of proposed SRAM as compared to a conventional 6T SRAM cell is 40.4%, compared to NC-SRAM cell is 12.4% and the total power dissipation of proposed SRAM as compared to a conventional 6T SRAM cell is 31.24%, compared to NC-SRAM cell is 10.4%. The SVN SINM WTV and WTI of proposed SRAM cell was also improved by 11.17%, 52.30%, 2.15%, 59.1% respectively as compare to 6T SRAM cell and as compare to NC-SRAM cell is 27.26%, 47.44%, 4.31%, 64.44% respectively. It can be found that the proposed cell is taking 28.6% extra area from the conventional SRAM cell whereas it is almost same with NC-SRAM cell.

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